DS33Z11DK
Ethernet Transport Design Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS33Z11 design kit is an easy-to-use evaluation board for the DS33Z11 Ethernet transport-over-serial link device. The DS33Z11DK is intended to be used with a resource card for the serial link. The serial link resource cards are complete with transceiver, transformers, and network connections. Dallas' ChipView software is provided with the design kit, giving point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal, queue overflow, Ethernet link, Tx/Rx, and interrupt status.

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ORDERING INFORMATION

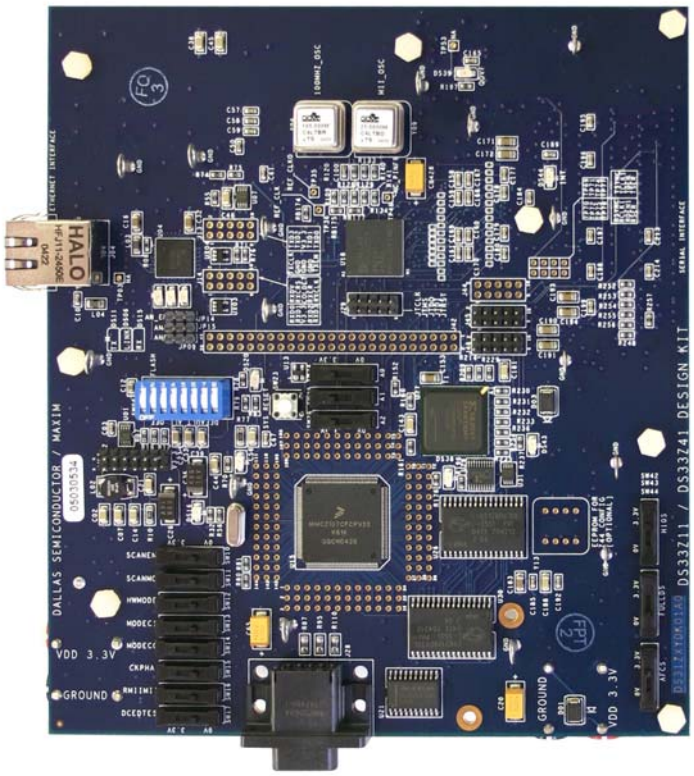
PART	DESCRIPTION
DS33Z11DK	DS33Z11 demo card, T3/E3, T1/E1 (SCT/LIU) resource card included

FEATURES

- Demonstrates Key Functions of DS33Z11 Ethernet Transport Chipset
- Includes Resource Card with DS21348 LIU, DS2155 T1E1 SCT, and DS3170 T3E3 SCT, Transformers, BNC and RJ48 Network Connectors and Termination
- Provides Support for Hardware and Software Modes
- On-Board MMC2107 Processor and ChipView Software Provide Point-and-Click Access to the DS33Z11, DS2155, and DS3170 Register Sets
- All DS33Z11 Interface Pins are Easily Accessible for External Data Source/Sink
- LEDs for Loss-of-Signal, Queue Overflow, Ethernet Link, Tx/Rx, and Interrupt Status
- Easy-to-Read Silk Screen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs

DESIGN KIT CONTENTS

- DS33Z11DK Main Board
- Single-Port Serial Card with DS2155 T1/E1 SCT, DS21348 T1/E1 LIU, and DS3170 T3/E3 SCT
- CD_ROM
  - ChipView Software and Manual
  - DS33Z11DK Data Sheet
  - Configuration Files



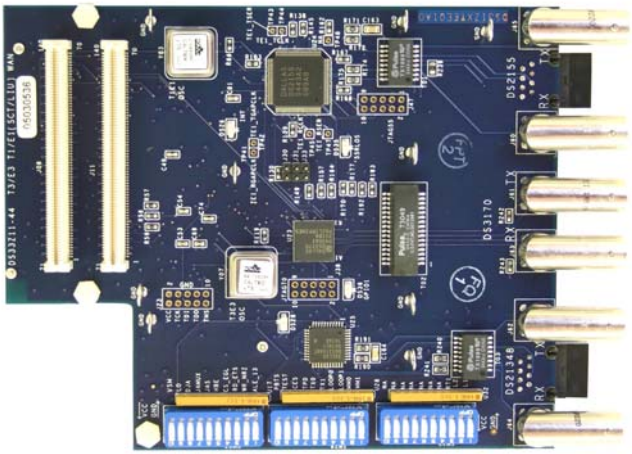


TABLE OF CONTENTS

GENERAL DESCRIPTION 1

ORDERING INFORMATION 1

DESIGN KIT CONTENTS 1

COMPONENT LIST 3

SYSTEM FLOORPLAN 8

PC BOARD ERRATA 8

FILE LOCATIONS 8

BASIC OPERATION 9

POWERING UP THE DESIGN KIT 9

General 9

BASIC DS33Z11 INITALIZATION (USED FOR ALL QUICK SETUPS) 9

Quick Setup #1 (Device Driver + CPLD Loopback) 9

Quick Setup #2 (DS21348 T1E1) 10

Quick Setup #3 (DS2155 T1E1) 10

Quick Setup #4 (DS3170 T3E3) 10

CONFIGURATION SWITCHES AND JUMPERS 11

ADDRESS MAP (ALL CARDS) 13

DS33Z11 INFORMATION 13

DS33Z11DK INFORMATION 13

TECHNICAL SUPPORT 13

SCHEMATICS 14

COMPONENT LIST

Table 1 shows the component list for the DS33Z44 and DS33Z11/DS33Z41 design kits and resource cards. This BOM contains the part listing for five boards. These boards are the DS33Z11DK, DS33Z44DK, DS21458RC, DS3174RC, and DS2155-DS21348-DS3170RC. Each reference designator is only used once. For example, U18 only appears on the DS33Z11DK and is not used on any of the other boards. See Table 2.

Table 1. Component List (Decoupling Caps Not Shown)

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
U18	1	ELITE 10/100 ETHERNET TRANSPORT OVER SERIAL LINK 14X14 CSBGA 169 PIN	Dallas Semiconductor	DS33Z11
U20	1	3.3V T1.E1.J1 QUAD TRANSCEIVER 0-70C 256P BGA	Dallas Semiconductor	DS21458
U22	1	QUAD 10/100 ETHERNET EXTENSION TO WAN 17X17 PBGA 256 PIN	Dallas Semiconductor	DS33Z44
U23	1	DS3/E3 SCT, 11X11 CSBGA, 100 PIN	Dallas Semiconductor	DS3170
U24	1	T1/E1/J1 XCVR 100P QFP 0-70C	Dallas Semiconductor	DS2156L
U25	1	3.3V LIU	Dallas Semiconductor	DS21348
UB08	1	QUAD TRIPLE DUAL SINGLE ATM PACKET PHYS FOR DS3 E3 STS1 0-70C 400P BGA	Dallas Semiconductor	DS3184
U01, U09	2	SOIC 8PIN STEP-UP DC-DC CONVERTER 0.5A LIMIT	Maxim	MAX1675EUA
U07, U11	2	8-Pin uMax SOIC 1.8V or Adj	Maxim	MAX1792EUA 18
U13, UB01	2	MICROPROCESSOR VOLTAGE MONITOR, 2.93V RESET, 4PIN SOT143	Maxim	MAX811SEU S-T
U21, UB07	2	Dual RS-232 transceivers with 3.3V/5V internal capacitors	MAXIM	NA
U31, UB06, UB11	3	8-Pin uMax SOIC 2.5V or Adj	Maxim	MAX1792EUA 25
C11, C13, C16, C25, C27, C31–C35, C37, C41, C47, CB10, CB63, CB114, CB128, CB164, CB496	19	1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M
CB390, CB391, CB395, CB396	4	1206 CERAM 0.1uF 25V 10%	Panasonic	ECJ-3VB1E104K
D01–D03, D05, DB03–DB05	7	SCHOTTKY DIODE, 1 AMP 40 VOLT	International Rectifier	10BQ040
DS01, DS07, DS10–DS12, DS17, DS20	7	LED, AMBER, SMD	Panasonic	LN1451C
DS02, DS03, DS09, DS14, DS15	5	L_LED, GREEN, SMD	Panasonic	LN1351C
DS04–DS06, DS08, DS13, DS16, DS18, DS27, DS28, DS35, DS37, DS38, DS40	13	LED, RED, SMD	Panasonic	LN1251C
DS19, DS43	2	LED, GREEN, SMD	Panasonic	LN1351C
DS21–DS26, DS30, DS32–DS34, DS36, DS39, DS41, DS42, DS44–DS48	19	L_LED, RED, SMD	Panasonic	LN1251C
GND_TP01–GND_TP07, GND_TP09—GND_TP44, GND_TP46–GND_TP68, GND_TPB01–GND_TPB10	76	STANDARD GROUND CLIP	KEYSTONE	4954

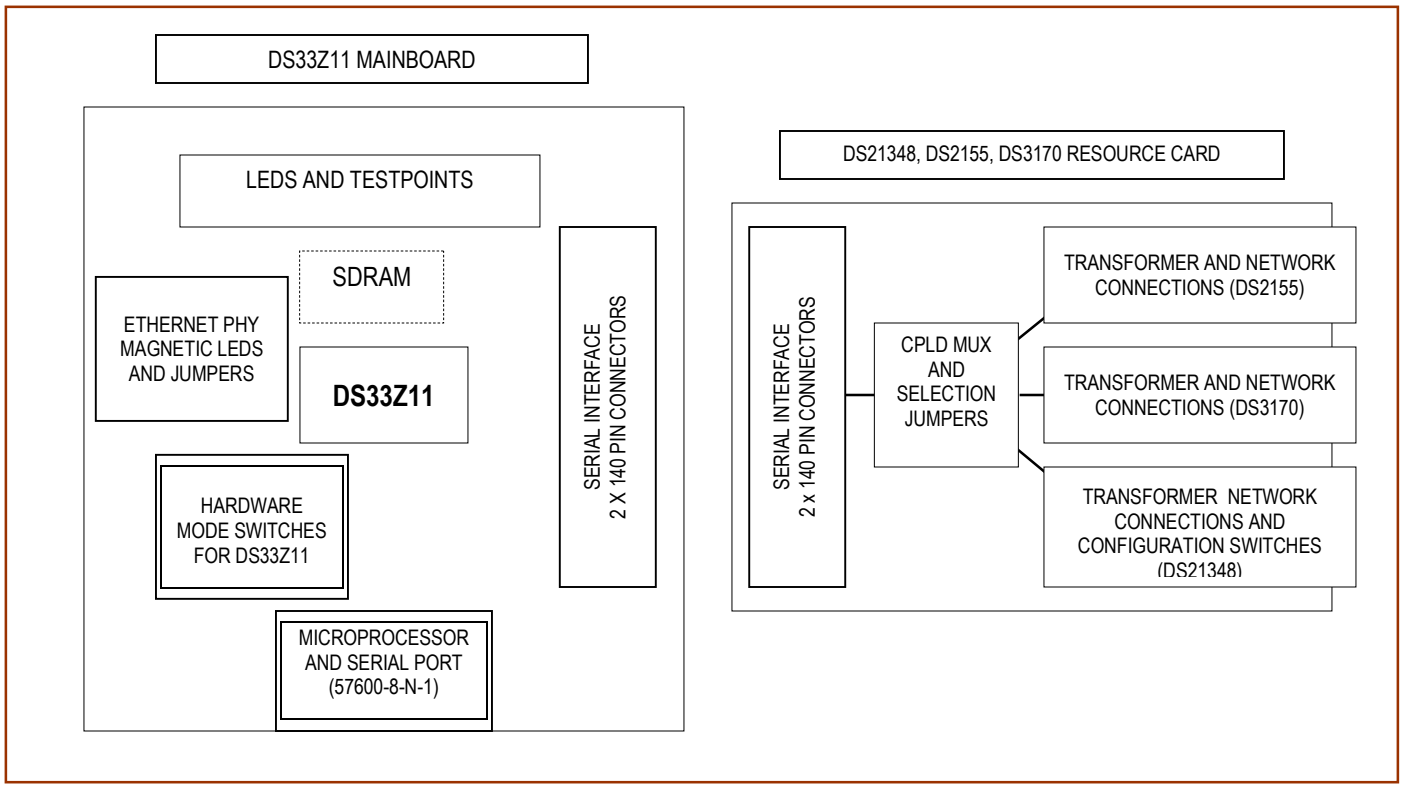
DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
H1–H8, H17–H19	8	KIT, 4-40 HARDWARE, .50 NYLON STANDOFF AND NYLON HEX-NUT	NA	Lab Stock
H9–H16	16	KIT, 4-40 HARDWARE, 1.12 NYLON STANDOFF AND NYLON HEX-NUT (1.12 STANDOFF PN = 4807K-ND)	NA	Lab Stock
J01–J05	5	CONNECTOR, FASTJACK SINGLE, 8 PIN	Halo Electronics	HFJ11-2450E
J06, J41	2	100 MIL 2*7 POS JUMPER	NA	Lab Stock
J07–J12	6	RECEPTACLE, SMD, 140 PIN, .8MM, 2 ROW VERTICAL	AMP	5-179010-6
J13–J22	10	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT DO NOT POPLUATE	NA	Lab Stock
J23, J29, J32, J38, J39, J43, J44, J47, JB07	9	L_TERMINAL STRIP, SHROUDED, 10 PIN, DUAL ROW, VERT	3M Electronics	2510-6002UB
J24, J30, J31, J33	4	100 MIL 2 POS JUMPER	NA	Lab Stock
J25, J26, J45, J46	4	TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	NA	Lab Stock
J27, J42	2	CONN 50 PIN, 2 ROW, POSTS VERT, MOTHERBOARD FOOTPRINT	SAMTEC	TSW-125-07-T-D
J28, J36	2	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
J48, J54, JB01	3	SOCKET, BANANA PLUG, HORIZONTAL, BLACK	Mouser Electronics	164-6218
J49–J52	4	CONNECTOR BNC 75 OHM VERTICAL 5PIN	Cambridge	CP-BNCPC-004
J53, JB02, JB08	3	SOCKET, BANANA PLUG, HORIZONTAL, RED	Mouser Electronics	164-6219
J55, JB11	2	L_RJ48 8 PIN SINGLE PORT CONNECTOR	MOLEX	15-43-8588
J56–J59, J61, J63	6	CONNECTOR BNC 75 OHM RA 5PIN	Trompetor	UCBJR220
J60, J62, J64, J65	4	CONNECTOR BNC RA 5PIN	Trompetor	UCBJR220
JB05, JB06, JB09, JB10, JB13, JB14	6	PLUG, SMD, 140 PIN, .8MM, 2 ROW VERTICAL	AMP	179031-6
JB12	1	RA RJ45 8PIN 4PORT JACK	MOL	43223-8140
JP01–JP19	19	100 MIL 3 POS JUMPER	NA	NA
L01, L03–L08, LB01, LB02	9	FERRITE 3A 100 OHM AT 100 MHZ 1206 SMD	Steward	HI1206N101R-00
L02, L09	2	INDUCTOR 22.0uH 2PIN SMT 20%	Coiltronics	UP1B-220
L10	1	XFMR 1-2CT XMIT, 1-1CT RCV, 40P WIDE SOIC	Pulse	T1068
R01, R02, RB10, RB11, RB18, RB19, RB22, RB23, RB26, RB27	10	RES 0603 54.9 Ohm 1/16W 1%	Panasonic	ERJ-3EKF54R9V
R03, R04, RB12, RB13, RB20, RB21, RB24, RB25, RB28, RB29	10	RES 0603 49.9 Ohm 1/16W 1%	Panasonic	ERJ-3EKF49R9V
R05, R06, R08, R09, R11	5	RES 0603 10.0K Ohm 1/16W 1% - Must be 1% tolerance	Panasonic	ERJ-3EKF1002V
R07, R12, R16, R79, R160, R244, R248, R250, R251, R254, R255, RB126, RB143, RB147, RB150, RB157	16	RES 0603 1.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ102V
R10, R107	2	RES 1206 5.6 Ohm 1/8W 5%	Panasonic	ERJ-

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
				8GEYJ5R6V
R132, R137, R142, R144, R156, RB194, RB208, RB227	8	L_RES 0603 0 Ohm 1/16W 1%	AVX	CJ10-000F
R13–R15, R18–R20, R22, R23, R29, R30, RB01, RB03, RB07, RB09, RB15–RB17, RB30–RB32, RB34–RB38, RB41, RB44, RB47, RB48, RB50–RB52, B55, RB60, RB62, RB72, RB73, RB75, RB80, RB82	40	RES 0603 5.1K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ512V
R17, R21, R25–R28, R31, R55, R57–R59, R71, R74–R76, R83, R96–R102, R105, R106, R109, R111, R112, R115–R117, R120, R122–R126, R128, R133, R134, R140, R141, RB61, RB96, RB97, RB99, RB100, RB102–RB110, RB112, RB114–RB119, RB121, RB123–RB125, RB127, RB128, RB130, RB131, RB133, RB135–RB138, RB145, RB148, RB149, RB160, RB161, RB164, RB165, RB167–RB171, RB173–RB181, RB184, RB187, RB311, RB320, RB335, RB339, RB359	104	RES 0603 30 Ohm 1/16W	Panasonic	ERJ-3GEYJ300V
R171, R172, R174, R175, R190, R191, R240, R241	8	L_RES 0805 0.0 Ohm 1/10W 5%	Panasonic	ERJ-6GEY0R00V
R198–R200, R210–R213, RB306, RB325, RB326	10	RES 0603 332 Ohm 1/16W 1%	Panasonic	ERJ-3EKF3320V
R201–R208, RB321–RB324, RB327–RB330	16	RES 1206 0 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ0R00V
R239, RB349	2	RES 0805 51.1 Ohm 1/10W 1%	Panasonic	ERJ-6ENF51R1V
R24, R114, R197, RB14, RB33, RB40, RB42, RB43, RB49, RB53, RB54, RB57–RB59, RB71, RB77, RB78, RB152–RB156, RB221, RB234, RB251, RB284, RB304, RB331, RB332, RB342, RB344, RB350, RB354, RB360	34	L_RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
R242, R243, RB144, RB166, RB355–RB358, RB368–RB371	12	RES 0603 51 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ510V
R32, R70, R78, R161, R176, R194, R195, R237, R238, RB129, RB134, RB146, RB193	13	RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
R33–R54, R60–R69, R72, R73, R131, R136, R143, R147, R150, R154, R158, R163, R166, R169, R173, R178–R189, R215–R228, RB89–RB95, RB101, RB188–RB191, RB196–RB199, RB202–RB205, RB210–RB213, RB216–RB219, RB223–RB226, RB230–RB233, RB239–RB242, RB244–RB249, RB252–RB260, RB265–RB268, RB270-RB282, RB289–	152	RES 0402 30 Ohm 1/16W 5%	Panasonic	ERJ-2GEJ300X

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
RB297				
R56, R90	2	RES 0603 1.0M Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ105V
R77, RB159	2	L_RES 1206 0 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ0R00V
R80, R81, R84, R87, R89, R91–R93, R95, R108, R110, R118, R127, R152, R153, R196, R209, R214, R229–R236, RB200, RB237, RB238, RB263, RB264, RB286, RB287, RB300, RB301, RB333, RB364	37	RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
R85, R88, R94, R104, R113, RB02, RB04–RB06, RB08, RB39, RB45, RB46, RB56, RB63–RB70, RB76, RB83, RB98, RB183, RB185, RB192, RB209, RB228, RB302, RB303, RB305, RB338, RB340, RB341, RB346–RB348, RB351–RB353, RB361–RB363, RB365–RB367	48	RES 0603 2.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ202V
R86, R103, R119, R121, R129, R130, R135, R138, R139, R145, R146, R149, R151, R157, R162, R164, R167, R168, R170, R177, R192, R193, R245-R247, R249, R252, R253, R256, R257, RB74, RB79, RB132, RB139-RB141, RB151, RB162, RB163, RB172, RB182, RB186, RB206, RB207, RB214, RB215, RB220, RB222, RB229, RB235, RB236, RB243, RB250, RB261, RB262, RB269, RB308–RB310, RB343, RB345	61	L_RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
RB201, RB285	2	RES 0805 330 Ohm 1/10W 5%	Panasonic	ERJ-6GEYJ331V
RB283	1	RES 0603 10K Ohm 1/10W 5% - SEE SPECIAL INSTRUCTIONS	Panasonic	603_ERJ-3GEYJ103V
RB298, RB299, RB312–RB319, RB336, RB337	12	RES 0805 61.9 Ohm 1/10W 1%	Panasonic	ERJ-6ENF61R9V
RB81, RB84–RB88, RB111, RB113, RB120, RB122	10	RES 0603 DO NOT POPULATE	NA	NA
SW01–SW05, SW08–SW21, SW24–SW26, SW29–SW31, SW33–SW44	37	L_SWITCH, SP3T SLIDE, 4PIN TH	Tyco	3-1437575-3
SW06, SW22	2	L_SWITH 8POS 16PIN DIP LOW PROFILE	AMP	435668-7
SW07, SW23	2	SWITCH MOM 4PIN SINGLE POLE	Panasonic	EVQPAE04M
SW27, SW28, SW32	3	L_DIPSWITCH, 10 POS	AMP	435668-9

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
T01, T03	2	XFMR 16P SMT	Pulse	TX1099
T02, TB01	2	XFMR, OCTAL T3/E3, 1 TO 2, SMT 32 PIN	Pulse	T3049
TP01–TP78, TPB01, TPB02	80	TESTPOINT, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U02–U06	5	IC, DsPHYTER11-SINGLE 10/100 ETHERNET TRANSCEIVER, 65 PIN LLP	National Semiconductor	DP83847ALQA56A
U08, U12, U29	3	1MBit Flash based config mem	Avnet	XCF01SV020C
U10	1	XILINX SPARTAN xc200 2.5V FPGA,256 PIN BGA	Xilinx	XC2S200-5FG256C
U14, U26, U30, UB05	4	CYPRESS SRAM, LAB STOCK	NA	NA
U15, U19	2	mmc2107 processor	Motorola	MMC2107
U16, U27	2	XILINX SPARTAN 2.5V FPGA,256 PIN BGA	Xilinx	XC2S50-5FG256C
U17, U28, U32	3	10 pin res pack, 10K ohm	NA	NA
UB02, UB03, UB04	3	100 PIN CPLD	XILINX	XC95144XL-10TQ100C
UB09, UB10	2	SYNCHRONOUS DRAM, 1MEGX32X4 BANKS, TSOP 86 PIN	Micron	MT48LC4M32B2TG-7
UX01–UX12, UXB02–UXB04, UXB06–UXB08	18	HIGH SPEED BUFFER	Fairchild	NC7SZ86
UXB01, UXB05	2	HIGH SPEED INVERTER	Fairchild	NC7SZ86
X01, X02	2	XTAL LOW PROFILE 8.0MHZ	ECL	EC1-8.000M
Y01, Y09	2	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 25.000 MHZ, Low Jitter required for PHY	SaRonix	NTH089AA3-25.000
Y02, Y13	2	SPI SERIAL EEPROM 16K 8 PIN DIP 2.7V NEEDS SOCKET	Atmel	AT25160A-10PI-2.7
Y03	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3-2.0480
Y05, Y06	2	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 100.000 MHZ	SaRonix	NTH089A3-100.0000
Y07	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 44.736 MHZ	SaRonix	NTH089AA3-44.736
Y08	1	OSCILLATOR, CRYSTAL CLOCK, 5.0V - 44.736 MHZ	SaRonix	NTH089AA-44.736
YB02	1	L_OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3-2.0480

SYSTEM FLOORPLAN



PC BOARD ERRATA

- Silk screen for the serial resource card has VCC and ground indicators pointing the wrong direction for configuration switches SW27, SW28, and SW32. This should be corrected with an adhesive label.
- Signal descriptions for JTAG connector are incorrect on the quad T1E1 card. This should be corrected with an adhesive label.

FILE LOCATIONS

This design kit relies upon several supporting files, which are provided on the CD and are available as a zip file from the Maxim website at www.maxim-ic.com/DS33Z11DK.

All locations are given relative to the top directory of the CD/zip file.

- DS33Z11 register definition files and configuration files:
  - .\cfg_demo_gui\DS33Z11_cfg_demo_gui\DS33Z11.def
  - .\DS33Z11_cfg_demo_gui\SU_LI_PORT1.def
  - .\DS33Z11_cfg_demo_gui\basic_config.mfg
- DS2155 register definition files and configuration files:
  - .\DS33Z11_cfg_demo_gui\te1_ds2155\DS2155.def
  - .\DS33Z11_cfg_demo_gui\te1_ds2155\e1_gapclk_crc4_hdb3_nocas.ini
- DS3170 register definition files and configuration files:
  - .\DS33Z11_cfg_demo_gui\te3_ds3170\ds3170_evbrd.def
  - .\DS33Z11_cfg_demo_gui\te3_ds3170\ds3_p1.def
  - ….. 6 other low level def files ….
  - .\DS33Z11_cfg_demo_gui\te3_ds3170\70_t3_sct_needscoaxlb.mfg

BASIC OPERATION

Powering Up the Design Kit

- Attach resource card to main board.
- Connect PCB 3.3V and GND banana plugs to power supply. At power-up the system should draw less than 1A.
- Set switches for software mode as described in Table 2 (short description follows).
  - Top bank all low (DCEDTE ….. SCANEN)
  - A2, A1, A0 in mid position, ScanTri low (right-hand side)
  - Bottom Bank all high (AFCS, FULLDS, H1OS)

General

- Upon power-up, the processor FPGA Status LEDs (DS43 green) will be lit. Interrupt LEDs (DS44 red) will not be lit. DS33Z11 Queue overflow LEDs (DS39 red) will not be lit. PHY LINK LED (DS06 green) should be lit if the Ethernet is connected.

Following are several basic system initializations.

Basic DS33Z11 Initialization (Used for All Quick Setups)

This section covers four basic methods for configuring the Z11. Any one of these initializations can be used with the following Quick Setup examples:

1. Upon power-up, the on-board device driver provides a basic configuration for the DS33Z11. This enables traffic to pass from the Ethernet port to the serial port. Consult the device driver documentation for further details. Device driver behavior is dependant upon jumper settings, which are detailed in Table 2.
2. Register-Based Configuration. Launch ChipView.exe and select *Register View.* When prompted for a definition file, pick the file named **DS33Z11.def**. After the definition file loads, go to the File menu and select File→Memory Config File→Load .MFG file. When prompted, select the file named **basic_config.mfg**.
3. Hardware Mode. Set switches as described in the section for powering up the design kit, then change the following: HWMODE←3.3V, A0←3.3VV, A1←3.3V, A2←0V. This sets the part for LSB first, scrambling off, HDLC encapsulated. At this point traffic will pass from the Ethernet port to the serial port. In this mode broadcast frames are not passed (i.e., ping).
4. EEPROM mode is available with the DK, but is beyond the scope of this manual.

Quick Setup #1 (Device Driver + CPLD Loopback)

- On the serial resource card install jumpers J30, J31, J33. This places the card in CPLD loopback as described in
- Table 3.
- Complete the hardware configuration and one of the basic DS33Z11 configurations as described in the previous section.
- Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
- At this point any packets sent to the DS33Z11 are echoed back. Incoming packets (i.e., ping) should cause the RX LED to blink, after which the TX LED should also blink.
- To interact with the device driver select from the drop down menu:
  - Tools→Plugins→Load Plugins. When asked if DLLs have already registered select yes
  - Select Tools→Plugins→DS33Z44/11/41 Device Driver Demo
  - A new form called ‘Zchip Configuration’ pops up.
  - Preload basic configuration for the GUI by selecting File→Load Settings (in the ‘Zchip Configuration’ form). Select the file named ‘basic_Config.eset’

Quick Setup #2 (DS21348 T1E1)

- On the serial resource card install jumper J30 (do not install J31 and J33). This places the card in DS21348 mode, with TCLK ←Osc Y03 as described in
- Table 3.
- Complete the hardware configuration and one of the basic DS33Z11 configurations as previously described.
- Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
- Set DS21348 configuration switches SW27, SW28, and SW32 in the ON position, and make the following changes:
  - Switch SW32: RT1, L2 and L1 OFF.
  - Switch SW28: PBTS OFF.
  - Switch SW27: WR_NRZ, HBE and L0 OFF.
- Place a loopback connector at the DS21348 network side; RLOS LED DS28 should go out.
- At this point any packets sent to the DS33Z11 are echoed back. Incoming packets (i.e., ping) should cause the RX LED to blink, after which the TX LED should also blink.

Quick Setup #3 (DS2155 T1E1)

- On the aerial resource card install jumper J31 (do not install J30 and J33). This places the serial card in DS2155 mode.
- Complete the hardware configuration and one of the basic DS33Z11 configurations as previously described.
- Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
- Launch ChipView.exe (or use existing session if its already open) and select *Register View.* When prompted for a definition file pick the file named **DS2155.def**. After the definition file loads, go to the File menu and select File→Reg Ini File→Load Ini File. When prompted, pick the file named **e1_gapclk_crc4_hdb3_nocas.ini**.
- Place a loopback connector at the DS2155 network side; RLOS LED DS35 should go out.
- At this point any packets sent to the DS33Z11 are echoed back. Incoming packets (i.e. ping) should cause the RX LED to blink, after which the TX LED should also blink.

Quick Setup #4 (DS3170 T3E3)

- On the serial resource card install jumper J33 (do not install J30 and J31). This places the card in DS3170 mode.
- Complete the hardware configuration and one of the basic DS33Z11 configurations as previously described.
- Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
- Launch ChipView.exe (or use existing session if its already open) and select *Register View.* When prompted for a definition file pick the file named **ds3170_evbrd.def**. After the definition file loads, go to the File menu and select File→Memory Config File→Load .MFG file. When prompted, select the file named **70_t3_sct_needscoaxlb.mfg**.
- Place a loopback connector at the DS3170 network side.
- At this point any packets sent to the DS33Z11 are echoed back. Incoming packets (i.e., ping) should cause the RX LED to blink, after which the TX LED should also blink.

CONFIGURATION SWITCHES AND JUMPERS

The DS33Z11DK has several configuration switches, banana plugs, oscillators, and jumpers. Table 2 provides a description of these signals, given in order of appearance on the PC board (going from left to right, top to bottom).

Table 2. Main Board PC Board Configuration

SILK SCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
J45.9 + J45.10	Reserved	Not installed	—	This jumper is not for use with the DS33Z11 design kit. Pin J45.10 has been removed to prevent accidental installation.
J45.7 + J45.8	Enable device driver	User decision	—	When installed the device driver will configure the DS33Z11 and the transceiver during power-up.
J45.5 + J45.6	Enable callbacks	User decision	—	When installed the driver will respond to interrupts.
GROUND (banana plug)	Power supply ground	—	—	System Ground. Always connected to power supply.
VDD 3.3V (banana plug)	Power supply VDD	—	—	System VDD. Always connected to power supply.
OnCe	BDM	—	—	Debug connector for processor
DCEDTES (3pos switch)	DS33Z11 mode pin; DTE/DCE selection	Low	Low	Low for DTE
RMIIMII (3pos switch)	DS33Z11 mode pin	Low	Low	High for RMII, low for MII
CKPHA (3pos switch)	DS33Z11 mode pin	Low	Low	SPI EEPROM hardware mode configuration switch
MODEC0 (3pos switch)	DS33Z11 mode pin	High	Low	Software mode selected
MODEC1 (3pos switch)	DS33Z11 mode pin	Low	Low	Software mode selected
HWMODE (3pos switch)	DS33Z11 mode pin	Low	Low	Hardware/software mode (software mode selected)
SCANMO (3pos switch)	DS33Z11 mode pin	Low	Low	Set low for normal operation
SCANEN (3pos switch)	DS33Z11 mode pin	Low	Low	Set low for normal operation
….testpoints….	DS33Z11 testpoints	—	—	Processor bus, JTAG and LAN side testpoints for Zchip
Z-RESET (button)	DS33Z11 reset	—	—	System reset
A2, A1, A0 (3 pos switches)	DS33Z11/SPI pins	Mid position	Mid position	Address pin/EEPROM config switch. Set to mid position to allow connection to processor.
SDRAM CLOCK	DS33Z11 SDRAM clock	Installed	installed	100MHz oscillator to drive SDRAM clock
MII CLOCK	PHY MII clock	Installed	installed	25MHz oscillator to drive SDRAM clock
spi_cs, spi_ck, spi_miso, spi_mosi	—	—	—	SPI signals (for EEPROM memory)
….testpoints…..	DS33Z11 testpoints	—	—	DS33Z11 serial port testpoints
AFCS	DS33Z11 mode pin	HW mode only	High	Set high to enable auto flow control.
FULLDS	DS33Z11 mode pin	HW mode only	High	Set high to enable full duplex.

SILK SCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
H10S	DS33Z11 mode pin	HW mode only	High	Set high to confg for 100Mb
GROUND/VDD (banana plug)	Power supply ground/3.3V	—	—	Redundant connection to system power. Use plugs at either top or bottom of board.
VDD 3.3V (banana plug)	Power supply VDD	—	—	Redundant connection to system power. Use plugs at either top or bottom of board.

Table 3. Serial Reference Card Jumper Settings

JUMPER SETTINGS	MODE	COMMENT
J30 Off, J31 Off, J33 Off	DS21348 Loop Timing	DS21348 TCLK is driven by DS21348 RCLK. This requires that the T1E1 device on the far end has its TCLK set to its local oscillator.
J30 Installed, J31 Off, J33 Off	DS21348 Source Timing	DS21348 TCLK is driven by Oscillator Y03. This requires that the T1E1 device on the far end has its TCLK set to its RCLK.
J30 Off, J31 Installed, J33 Off	DS2155 T1E1	TCLK source is determined by a register setting in the DS2155.
J30 Off, J31 Off, J33 Installed	DS3170 T3E3	TCLK source is determined by a register setting in the DS3170.
J30 Installed, J31 Installed, J33 Installed	CPLD loopback	CPLD loopback makes the following connections: Zrser ← Ztser, Ztden ← 3.3V, Zrden ← 3.3V, Ztclki ← OscY03, Zrclki ← OscY03

ADDRESS MAP (ALL CARDS)

Motorola resource card address space begins at 0x81000000. All offsets given below are relative to the beginning of the daughter card address space (shown previously).

Table 4. Overview of Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0087	FPGA	Processor board identification
0X1000 to 0X1FFF	DS33Z11	DS33Z11. Uses CS_X1.
0X2000 to 0X2FFF	DS2155	T1E1 portion of single T1E1–T3E3 WAN card. Uses CS_X2.
0X3000 to 0X3FFF	DS3170	T3E3 portion of single T1E1–T3E3 WAN card. Uses CS_X3.

Registers in the DS33Z11, DS2155, and DS3170 can be easily modified using the ChipView host-based user-interface software with the definition files previously mentioned.

DS33Z11 INFORMATION

For more information about the DS33Z11, consult the DS33Z11 data sheet available on our website at www.maxim-ic.com/DS33Z11.

DS33Z11DK INFORMATION

For more information about the DS33Z11DK, including software downloads, consult the DS33Z11DK data sheet available on the our website at www.maxim-ic.com/DS33Z11DK.

TECHNICAL SUPPORT

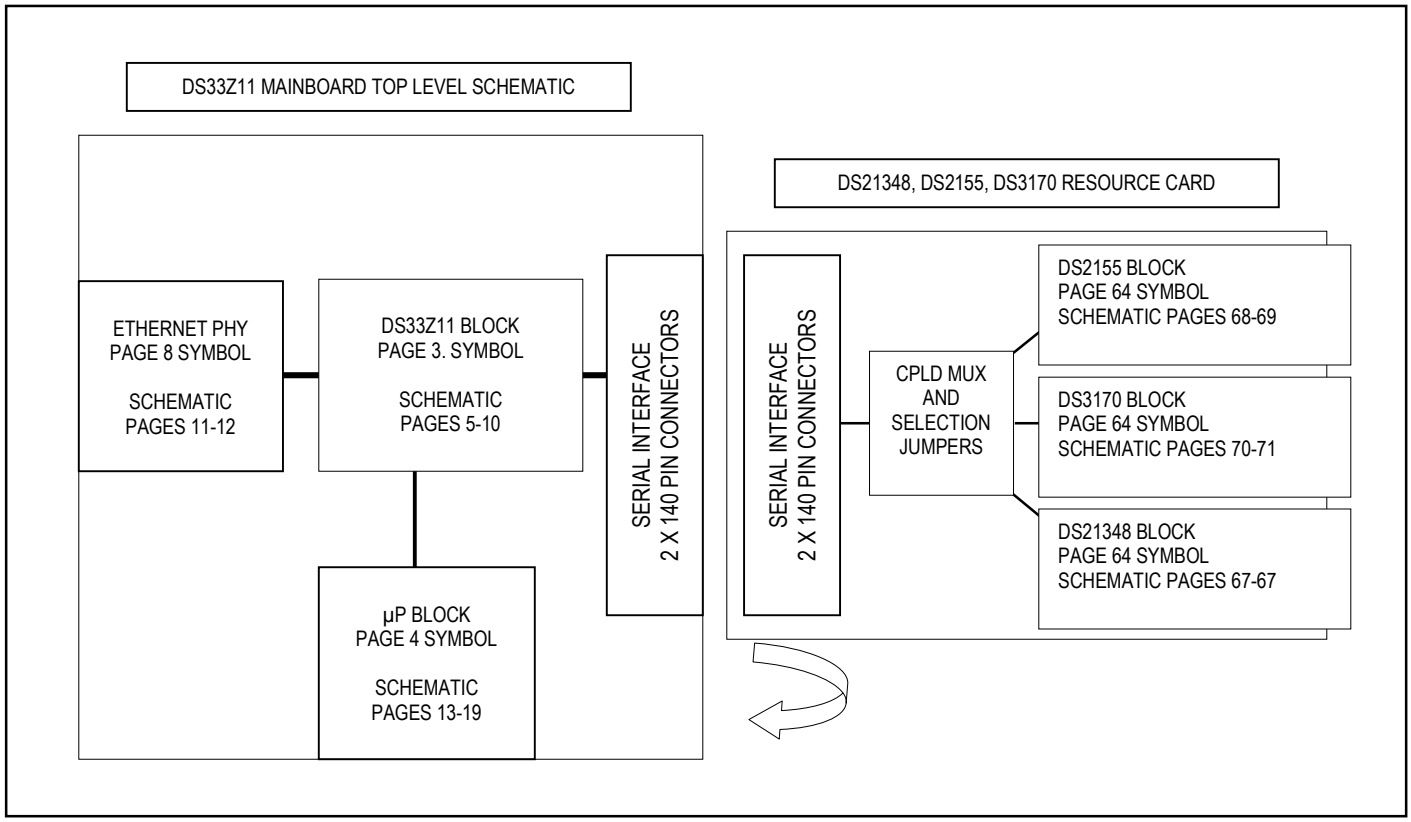
For additional technical support, please e-mail your questions to telecom.support@dalsemi.com.

SCHEMATICS

The DS33Z11DK schematics are featured in the following pages. As this is a hierarchal schematic some explanation is in order. The main board is composed of three hierarchal blocks: the processor block, the DS33Z11 block, and an Ethernet block inside the DS33Z11 block, which is a nested hierarchy block. The serial card consists of three hierarchy blocks, one for each of the DS21348, DS2155, and DS3170. These blocks are connected by the CPLD, which connects to the 140-pin AV bus, which snaps into the main board.

All signals inside a hierarchy block are local, with exception for V_{CC} and ground. In-port and out-port connectors are used to allow signals inside a hierarchy block to become accessible as pins on the hierarchy blocks symbol. From here blocks are wired together as if they were ordinary components. The system diagram is shown again below, with schematic page numbers given for each functional block.

This system contained other hierarchy blocks that are not shown (primarily quad-port serial cards and the DS33Z44 mainboard). Due to this page numbers will not be continuous and some gaps in numbering will be seen when referring to the total page count. However, page numbers inside any given hierarchy block will be continuous.



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CR-3 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_IS@_ZTOP_LIB\,_Z11TOP_DN\(SCH_1):PAGE1

DS33Z11 TOP LEVEL

V3_3

V3_3 3A5<> 3A8<> 3B5<> 3B8<> 3C5<> 3C8<> 4D8> 3D8 4D8

GND

HIERARCHICAL BLOCK

5C4v 5B1v 5A1v 4C6< A_DUT<9,,0> ADDR<9,,0>

5B4v 4C6< D_DUT<7,,0> DAT<7,,0>

5A6v 4D3> CS_X1 CS

5A5v 4C5< RD_DUT RD

5A5v 4C5< WR_DUT WR

5A5v 4C3> 3C7<> RESET_B RESET_B

6A6v 3C6<> Z41RSYNC Z41RSYNC

6A6v 3C6<> Z41TSYNC Z41TSYNC

INT INT2 3C7<> 3C8<> 4D5< 5A6v

_z11andlan_dn

PAGES 5-10

HWMODE BTS_DUT 4B5< 5A5v

MODEC0 BIS0_DUT 4C5< 5A5v

MODEC1 BIS1_DUT 4B5< 5A5v

RCLKI TCLKI RSER TSER RDEN TDEN

Z44_RCLK<1> Z44_TCLK<1> Z44_RSER<1> Z44_TSER<1> Z44_RDEN<1> Z44_TDEN<1>

3C6<> 5C5v 3C6<> 5D5v 3C6<> 5C4v 3C8<> 5C5v

PLUG

P2 CONNECTOR (PLUG)

JB13

VDD

GND INT5 4C5< INT2 3D1> 3C7<> 5A6v 4D5<

INT3 4D5< INT4 4C5<

INT2 3C8<> 3D1> 4D5< 5A6v

RESET_B 4C3> 3D3< 5A5v

Z44_RSER<1> 3C1> 5C5v

Z44_TSER<1> 3C1> 5D5v

SIG_RETURN 3A1> 3A3<> 3B7<>

Z44_RDEN<1> 3C1> 5C5v

Z44_TDEN<1> 3C1> 5C4v

Z44_RCLK<1> 3C2> 5C5v

Z44_TCLK<1> 3C2> 5C5v

Z41RSYNC 3D3< 6A6v

Z41TSYNC 3D3< 6A6v

4D8 3D8 3D8> 3B5<> 3A8<> 3A5<> 4D8> 3C8<> 3C5<> 3B8<>

Z44_RSER<2>

Z44_RDEN<2>

Z44_RCLK<2>

SIG_RETURN 3A1> 3A3<> 3C7<>

Z44_TSER<2>

Z44_TDEN<2>

Z44_TCLK<2>

TDO_NU 4B4>

TCK_NU 4B4>

TDI_NU 4B4> 3D8> 3C5<> 3D8

TMS_NU 4B4> 3C5<> 3D8

XA<15,,0>

OSC2_NU 3B8<> 3C8<> 3C5<> 3A6<> 3A5<> 3B8<> 3D8>

OSC4_NU 4D8 3D8 4D8> 3D8>

OSC3_NU

PLUG

P1 CONNECTOR (PLUG)

JB09

4C3> CS_X5

ALE

CS_X4 4C3>

Z44_RSER<3>

Z44_TSER<3>

Z44_RDEN<3>

Z44_TDEN<3>

Z44_RCLK<3>

Z44_TCLK<3>

Z44_RSER<4>

Z44_TSER<4>

Z44_RDEN<4>

Z44_TDEN<4>

Z44_RCLK<4>

SIG_RETURN 3A1> 3B7<> 3C7<>

Z44_TCLK<4>

3A4 4B2>

XD<7,,0>

OSC1_NU

4D3> CS_X2

4C3> CS_X3

4C3> WR_X

RW_X 4C3>

GND SIG_RETURN 3A3<> 3B7<> 3C7<>

MOTHERBOARD CONNECTORS FOR WAN R.C.

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:1/2<BLOCK> 3/71<TOTAL>

BLOCK NAME: _z11top_dn, PARENT BLOCK: _ztopdn_\

PRINTED Tue Feb 01 14:17:39 2005

V3_3

V3_3 3A5<> 3A8<> 3B5<> 3B8<> 3C5<> 3C8<> 3D8> 3D8 4D8

GND

I47

PAGES 13-19

_motprocrescard_dn

13B7v 3D1> 3C8<> 3C7<>	INT2	INT2	CS_X1	CS_X1	3D3< 17B3v	
13B7v 3C7<>	INT3	INT3	CS_X2	CS_X2	3A5<> 17B3v	
13B7v 3C7<>	INT4	INT4	CS_X3	CS_X3	3A5<> 17A4v	
14D4v 3C8<>	INT5	INT5	CS_X4	CS_X4	3C4<> 17A4v	
			CS_X5	CS_X5	3C5<> 17A4v	
			RESET_B	RESET_B	3C7<> 3D3< 13A5v	
17C3v 3D3<	RD_DUT	RD_DUT				
17C3v 3D3<	WR_DUT	WR_DUT				
17D5v 3D3<	D_DUT<7..0>	D_DUT<7..0>				
17A6v 17A5v 3D3<	A_DUT<11..0>	A_DUT<11..0>	RW_X	RW_X	3A4<> 17B3v	
17C3v 3C1>	BIS0_DUT	BIS0_DUT	WR	WR_X	3A5<> 17B3v	
17C3v 3C1>	BIS1_DUT	BIS1_DUT	XA<15..0>	XA<15..0>		3A7 3A8 17C7v
17C3v 3D1>	BTS_DUT	BTS_DUT	XD<7..0>	XD<7..0>		3A4 3A6 17B3v

TMS_NU TDI_NU TCK_NU TDO_NU

TMS_NU TDI_NU TCK_NU TDO_NU 3A8<> 19A7v 3A8<> 19A7v 3A7<> 19A7v

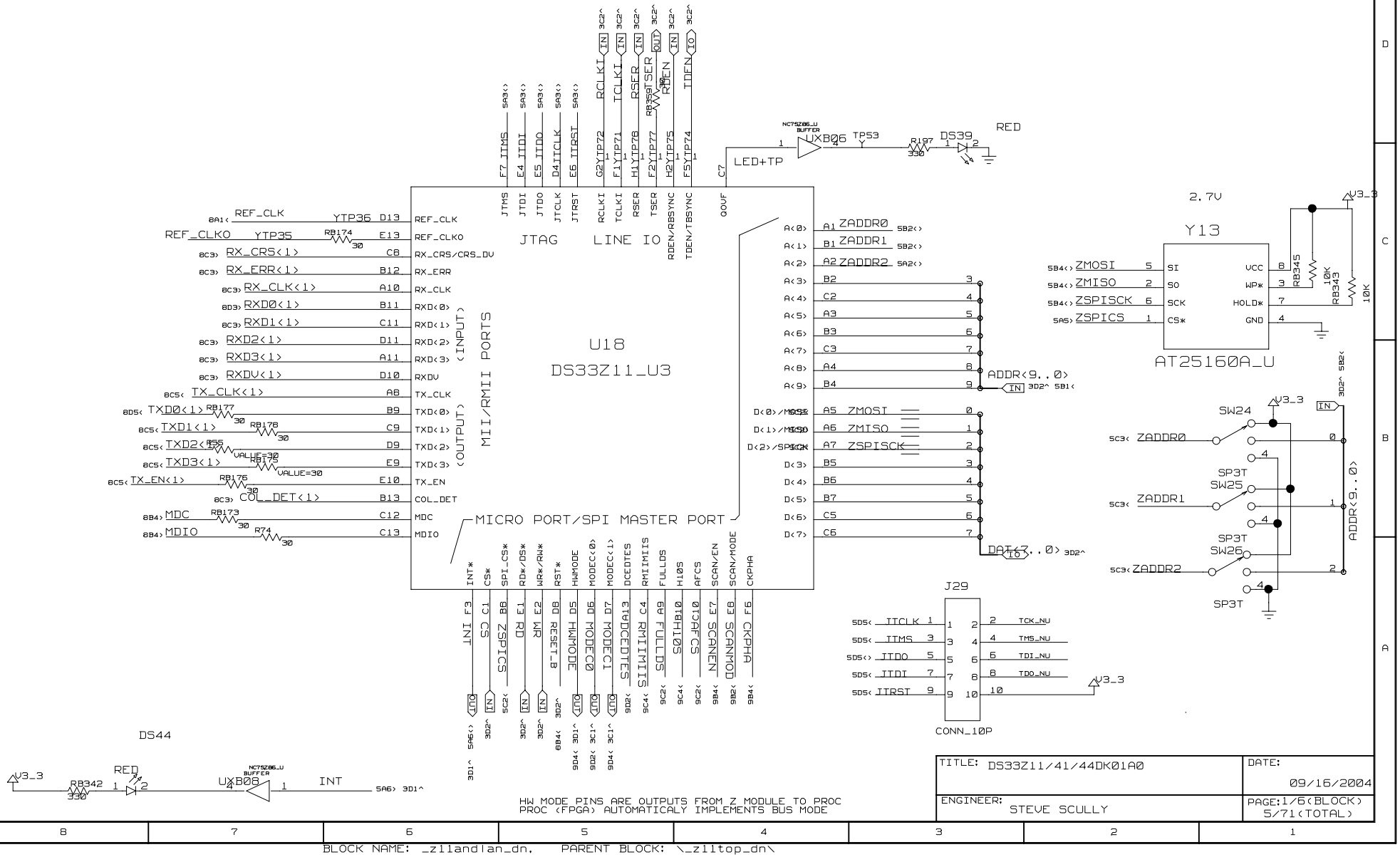
TITLE: DS33Z11/41/44DK01A0	DATE: 09/15/2004
ENGINEER: STEVE SCULLY	PAGE:2/2(BLOCK) 4/71(TOTAL)

BLOCK NAME: _z11top_dn, PARENT BLOCK: _ztopdn_\

JMP_3

CR-5 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_IS@_ZTOP_LIB\,_Z11TOP_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\,_Z11ANDLAN_DN\(SCH_1):PAGE1

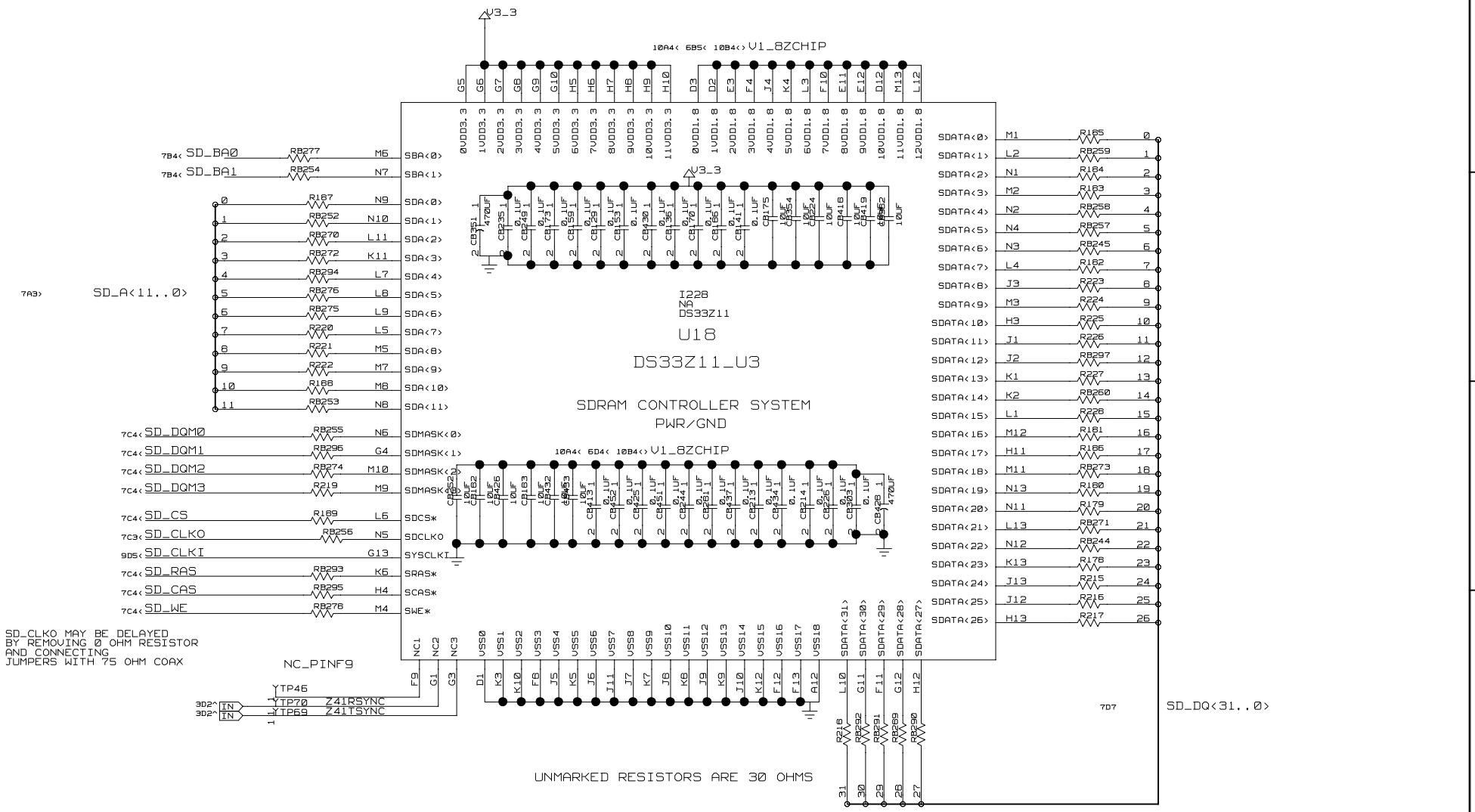
DS33Z11/Z41



HW MODE PINS ARE OUTPUTS FROM Z MODULE TO PROC
PROC (FPGA) AUTOMATICALY IMPLEMENTS BUS MODE

TITLE: DS33Z11/41/44DK01A0	DATE: 09/15/2004
ENGINEER: STEVE SCULLY	PAGE:1/6(BLOCK) 5/71(TOTAL)

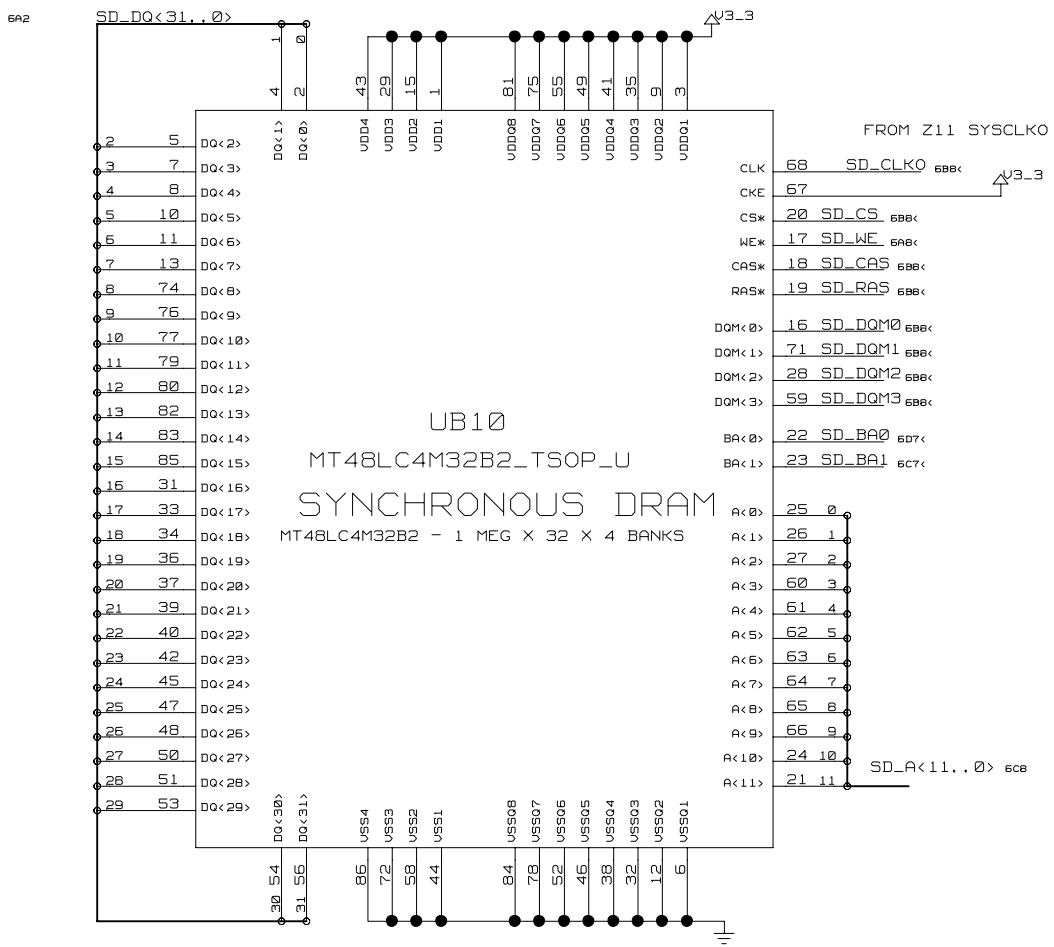
BLOCK NAME: _z11andlan_dn, PARENT BLOCK: _z11top_dn\



TITLE: DS33Z11/41/44DK01A0	DATE: 09/15/2004
ENGINEER: STEVE SCULLY	PAGE:2/6<BLOCK> 6/71<TOTAL>

BLOCK NAME: _z11andlan_dn, PARENT BLOCK: _z11top_dn\

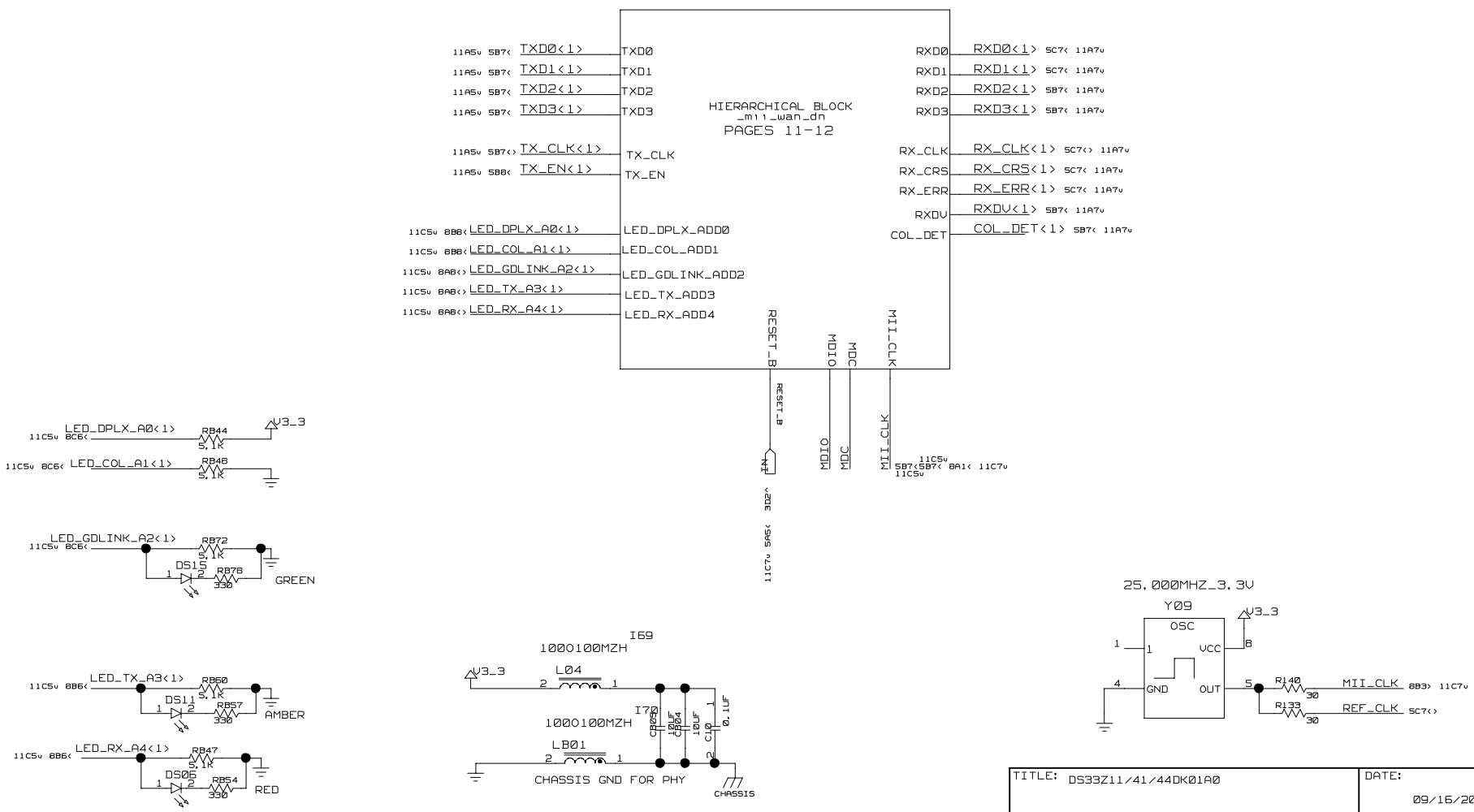
CR-7 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_IS@_ZTOP_LIB\,_Z11TOP_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\,_Z11ANDLAN_DN\(SCH_1):PAGE3



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:3/6(BLOCK) 7/71(TOTAL)

BLOCK NAME: _z11andlan_dn, PARENT BLOCK: _z11top_dn\

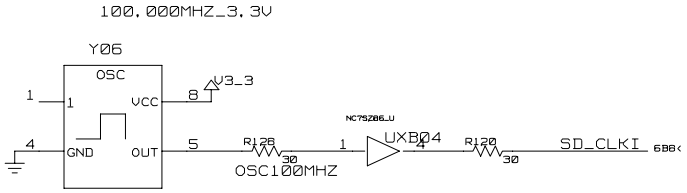
CR-8 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_I5@_ZTOP_LIB\,_Z11TOP_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\,_Z11ANDLAN_DN\(SCH_1):PAGE4

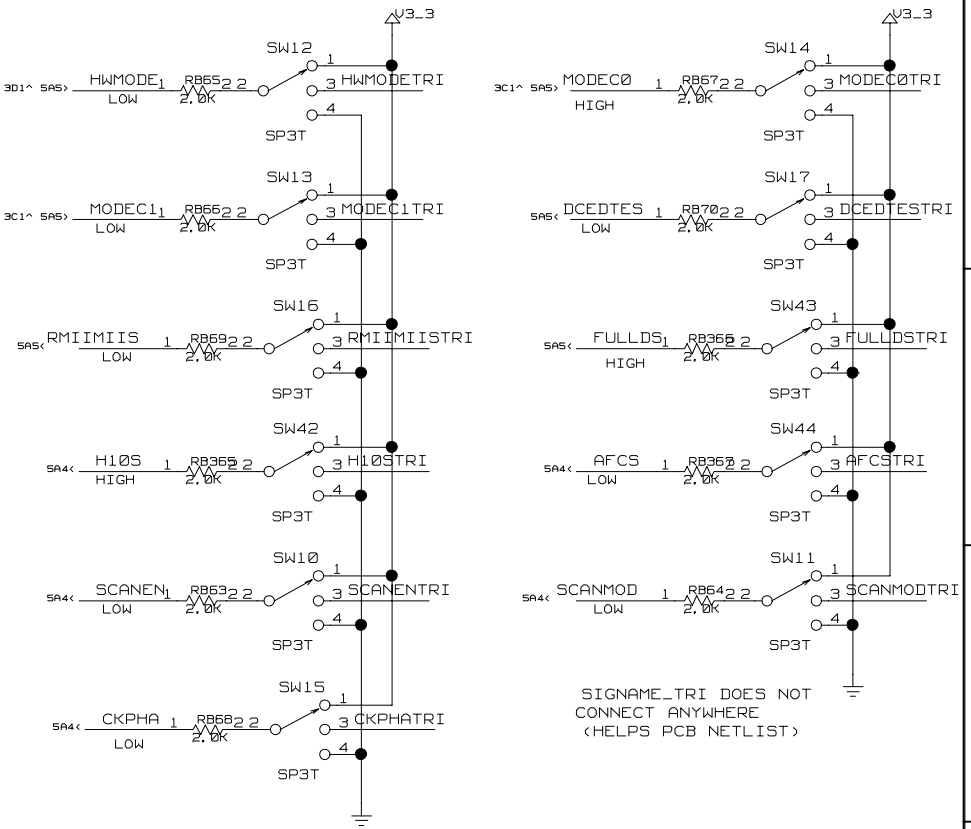


TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:4/6(BLOCK) 8/71(TOTAL)

BLOCK NAME: _z11andlan_dn, PARENT BLOCK: _z11top_dn\

CR-9 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_IS@_ZTOP_LIB\,_Z11TOP_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\,_Z11ANDLAN_DN\(SCH_1):PAGE5



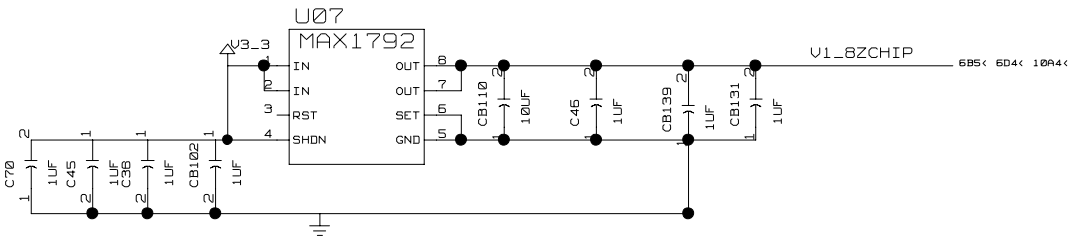


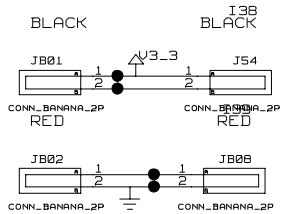
MODE (SHOWN BELOW SIGNAL) RESULTS IN:
MOTOROLA NON-MUX, MII, FULL DUPLEX, 100 MBIT, AUTO-FLOW CONTROL

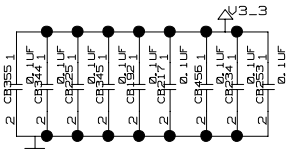
CONFIG SWITCHES FOR Z11

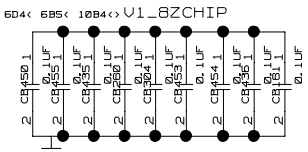
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:5/6(BLOCK) 9/71(TOTAL)

BLOCK NAME: _z11andlan_dn, PARENT BLOCK: _z11top_dn\



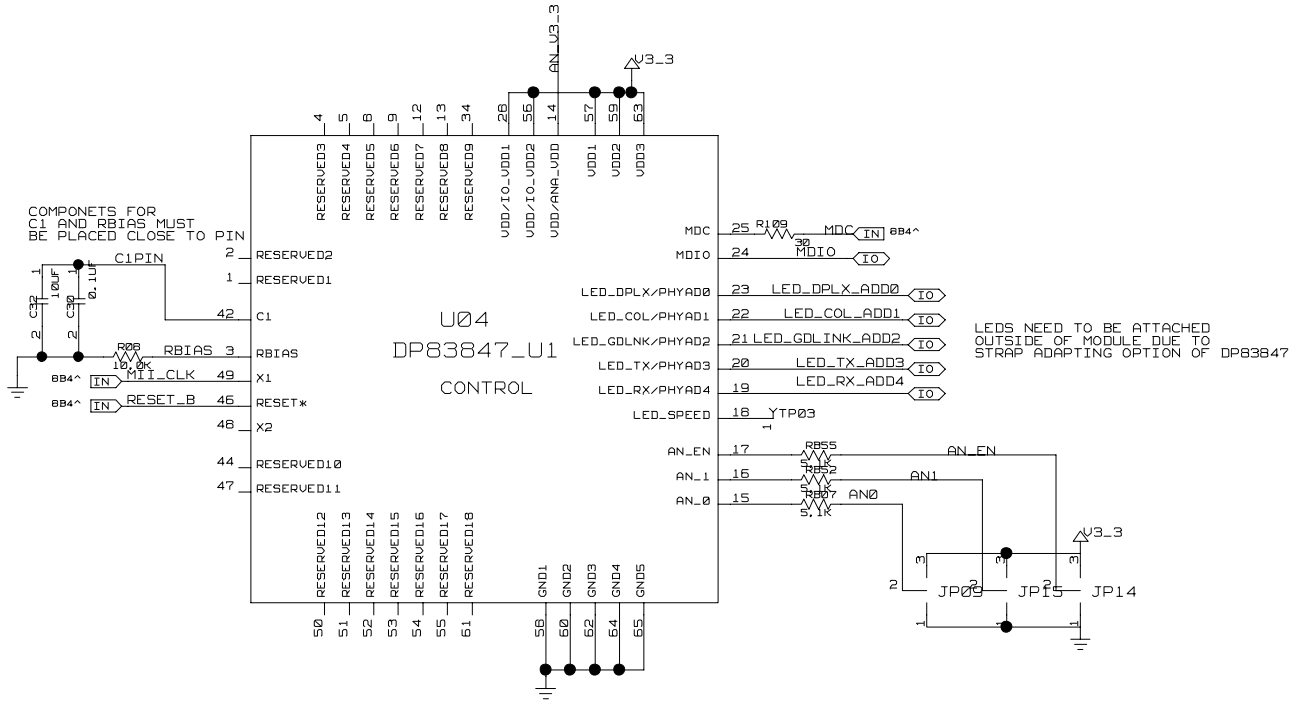


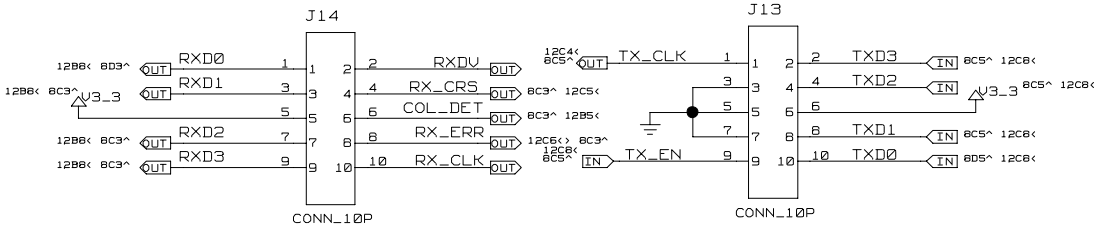


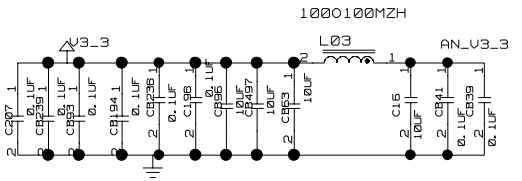


TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:6/6(BLOCK) 10/71(TOTAL)

BLOCK NAME: _z11andlan_dn. PARENT BLOCK: _z11top_dn\



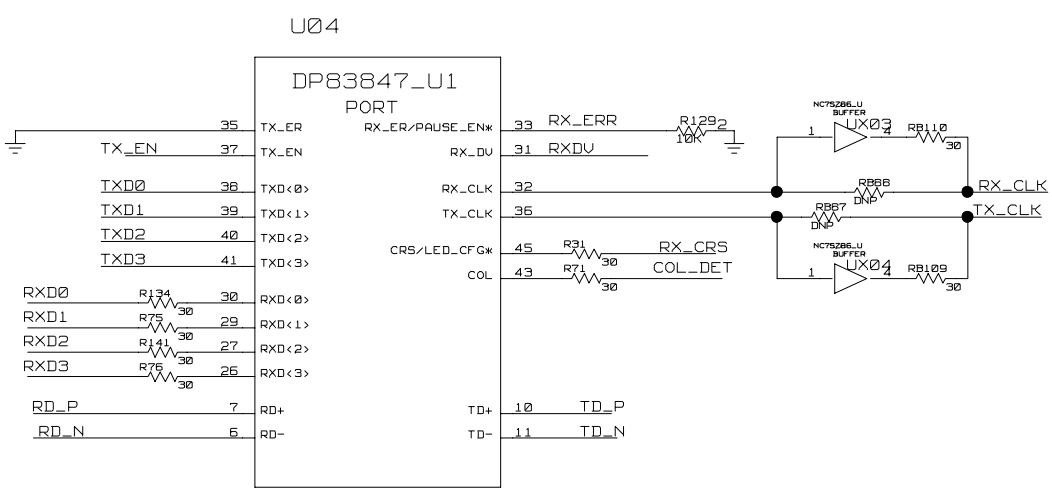


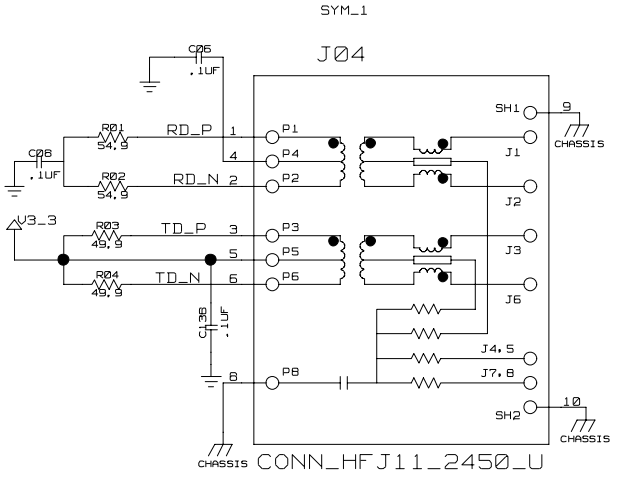


PLACEMENT NOTE:
TESTPOINTS (SHOWN ABOVE) MUST BE PLACED THE SAME FOR EACH PORT TO ALLOW USE OF A DIFFERENT PHY CARD IF DESIRED. PLACEMENT SHOULD ALLOW 0.2 BETWEEN CONNECTORS.

ON Z44 CARD ALL 4 PORTS MUST BE PLACED WITH EQUAL SPACING AND A COMMON CENTER LINE

TITLE: DS33Z11/41/44DK01A0	DATE: 09/15/2004
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 11/71(TOTAL)





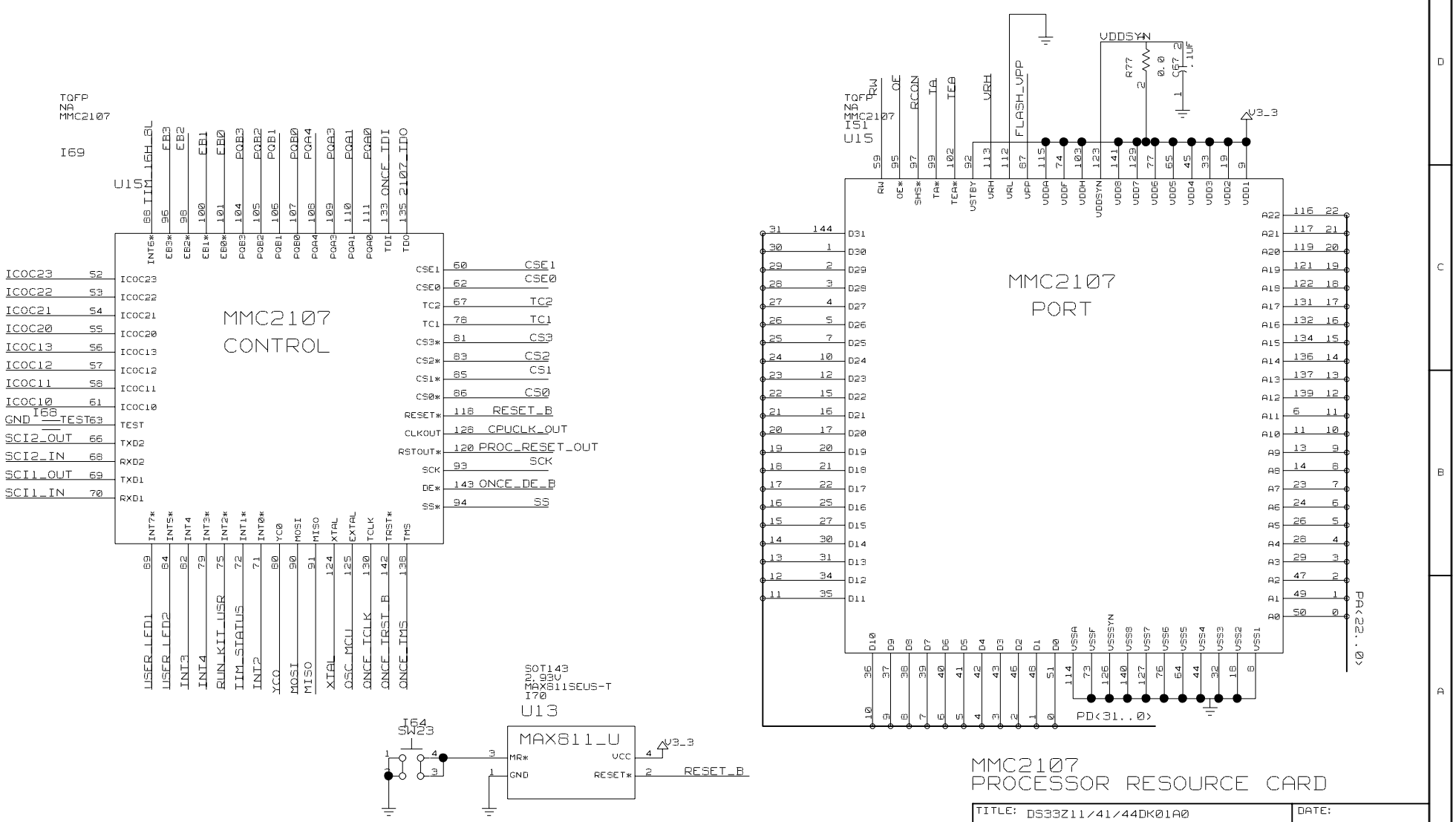
CAPS FOR XFRM CENTER TAP
SHOULD BE PLACED CLOSE TO XFRM

RESISTORS FOR TD+-/RD+-
SHOULD BE PLACED CLOSE TO PHY

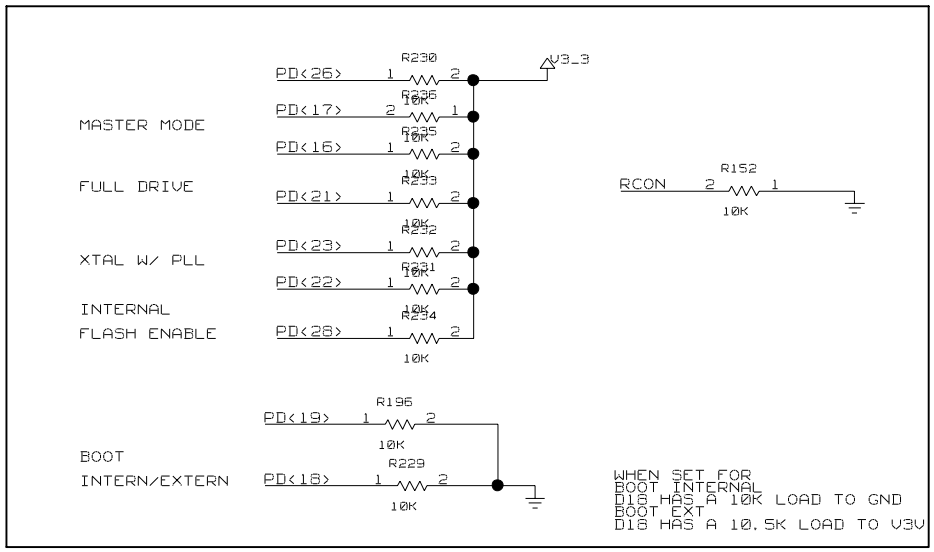
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:2/2(BLOCK) 12/71(TOTAL)

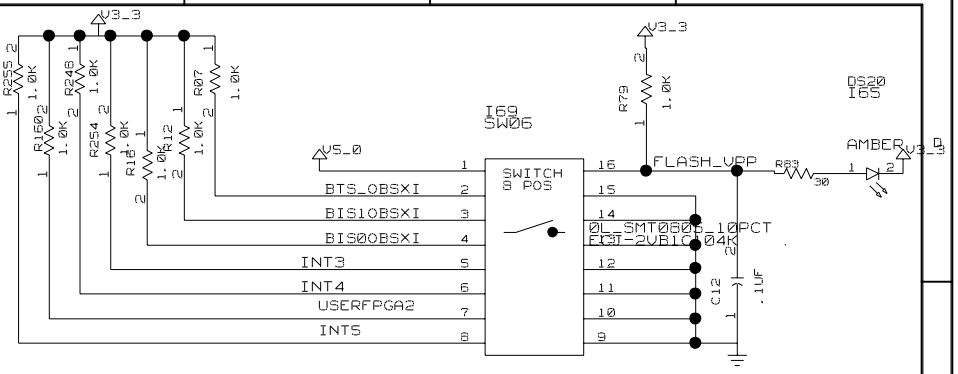
BLOCK NAME: _mii_wan_dn, PARENT BLOCK: _zllandlan_dn\

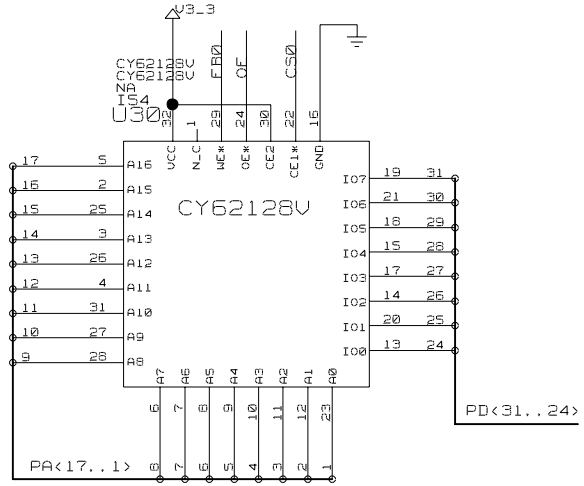
CR-13 : @_ztop_lib\,_ztopdn_\(sch_1):page1_15@_ztop_lib\,_zlltop_dn\(sch_1):page2_147@_ztop_lib\,_motprocrescard_dn\(sch_1):Page1

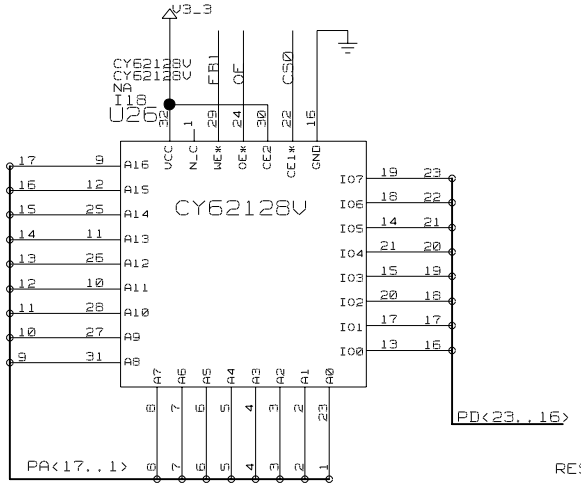


RESET CONFIGURATION





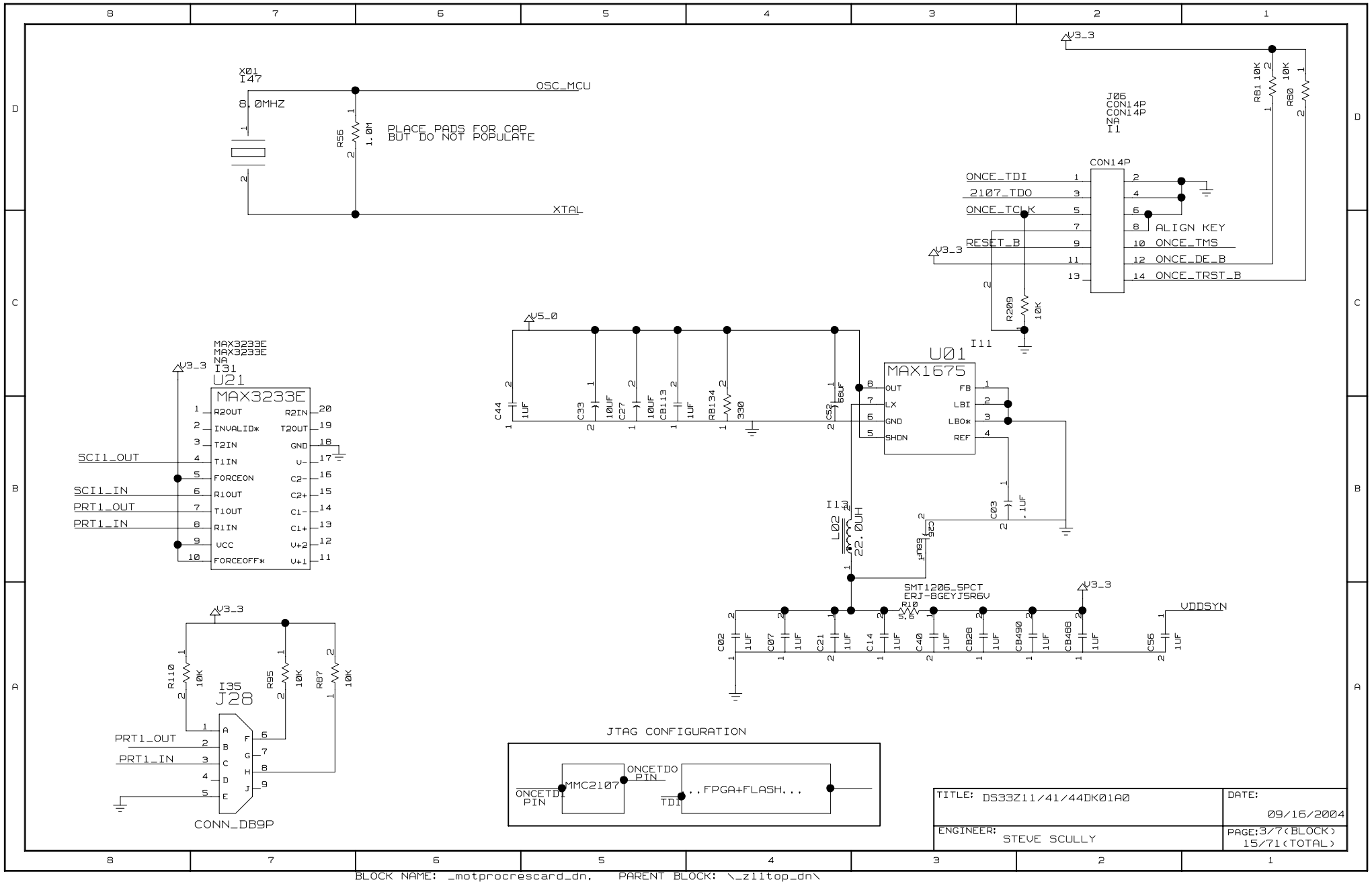




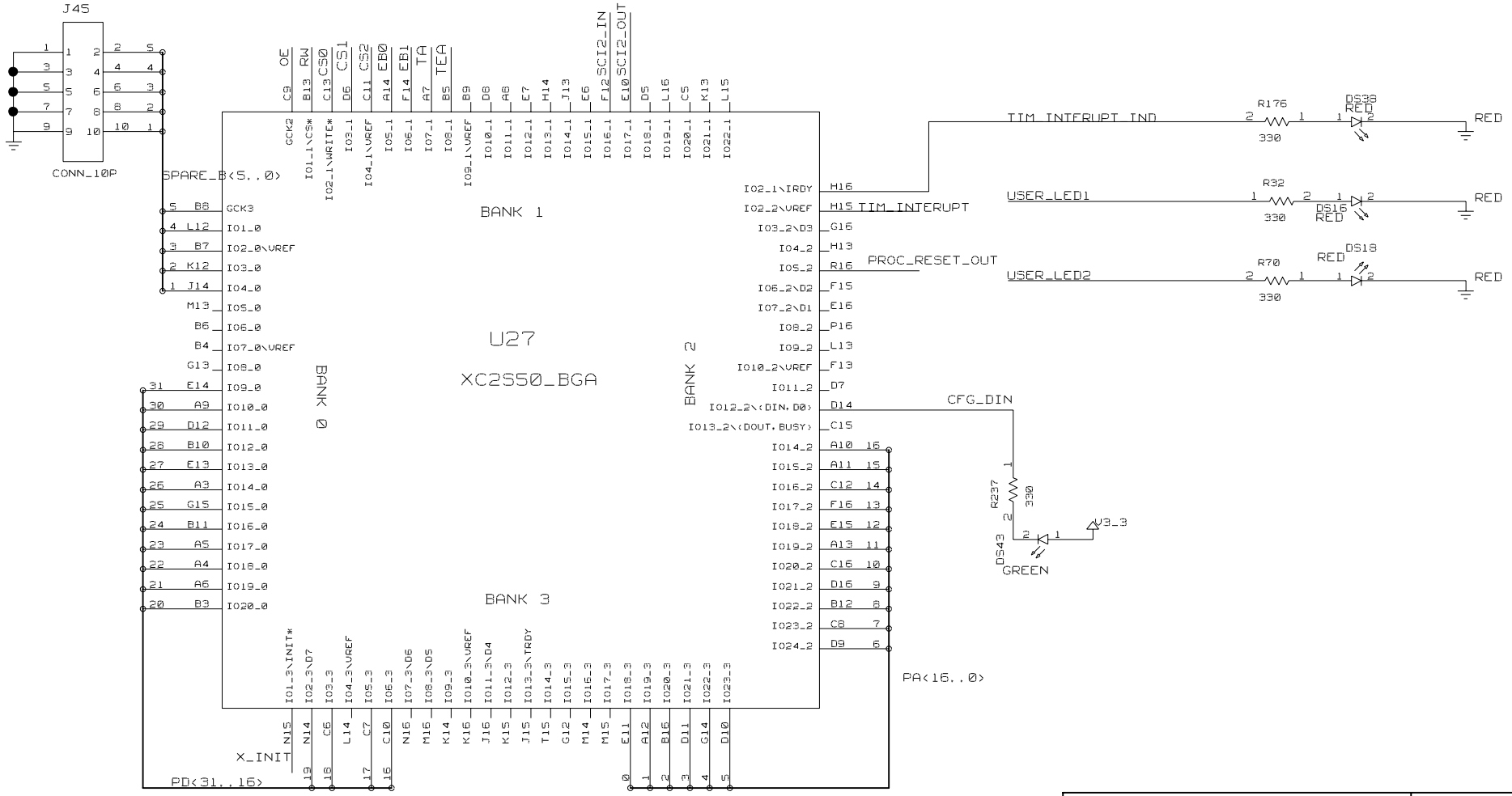
RESET AND CHIP CONFIGURATION

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:2/7(BLOCK) 14/71(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _zlltop_dn\

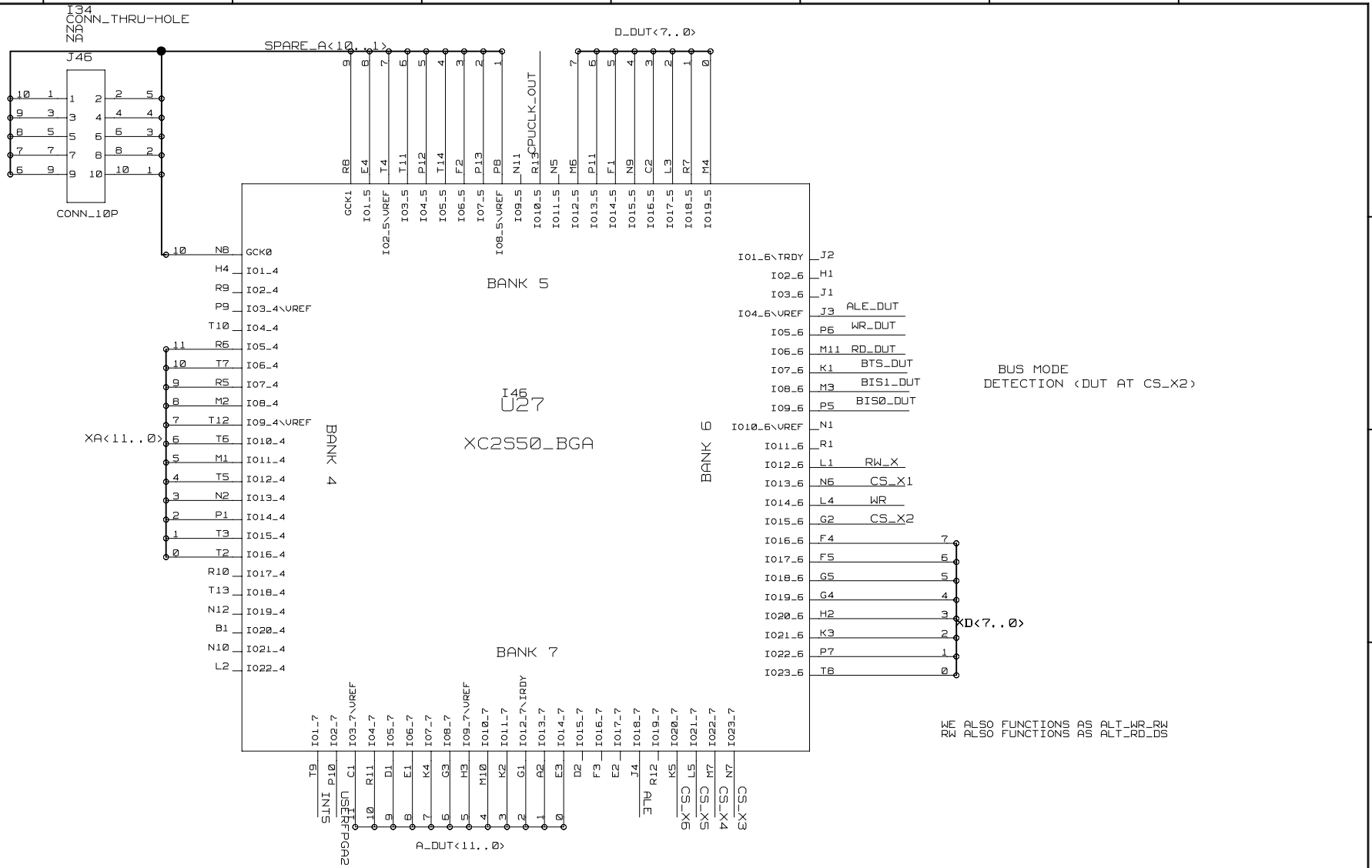


BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _z11top_dn\



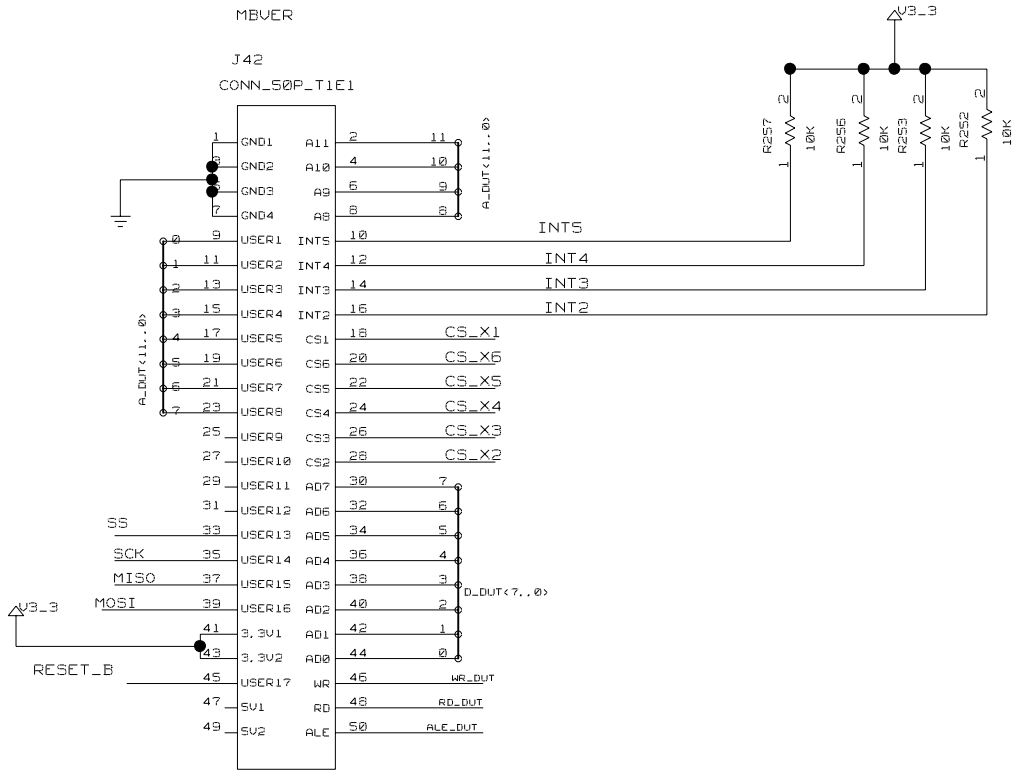
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:4/7(BLOCK) 16/71(TOTAL)

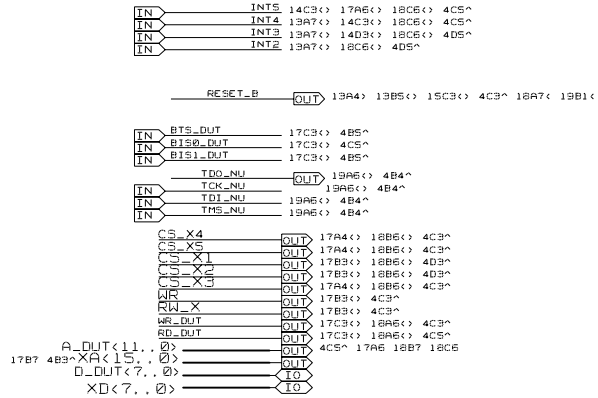
BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _zlltop_dn\



TITLE: DS33Z11/41/44DK01A0	DATE: 09/15/2004
ENGINEER: STEVE SCULLY	PAGE:5/7(BLOCK) 17/71(TOTAL)

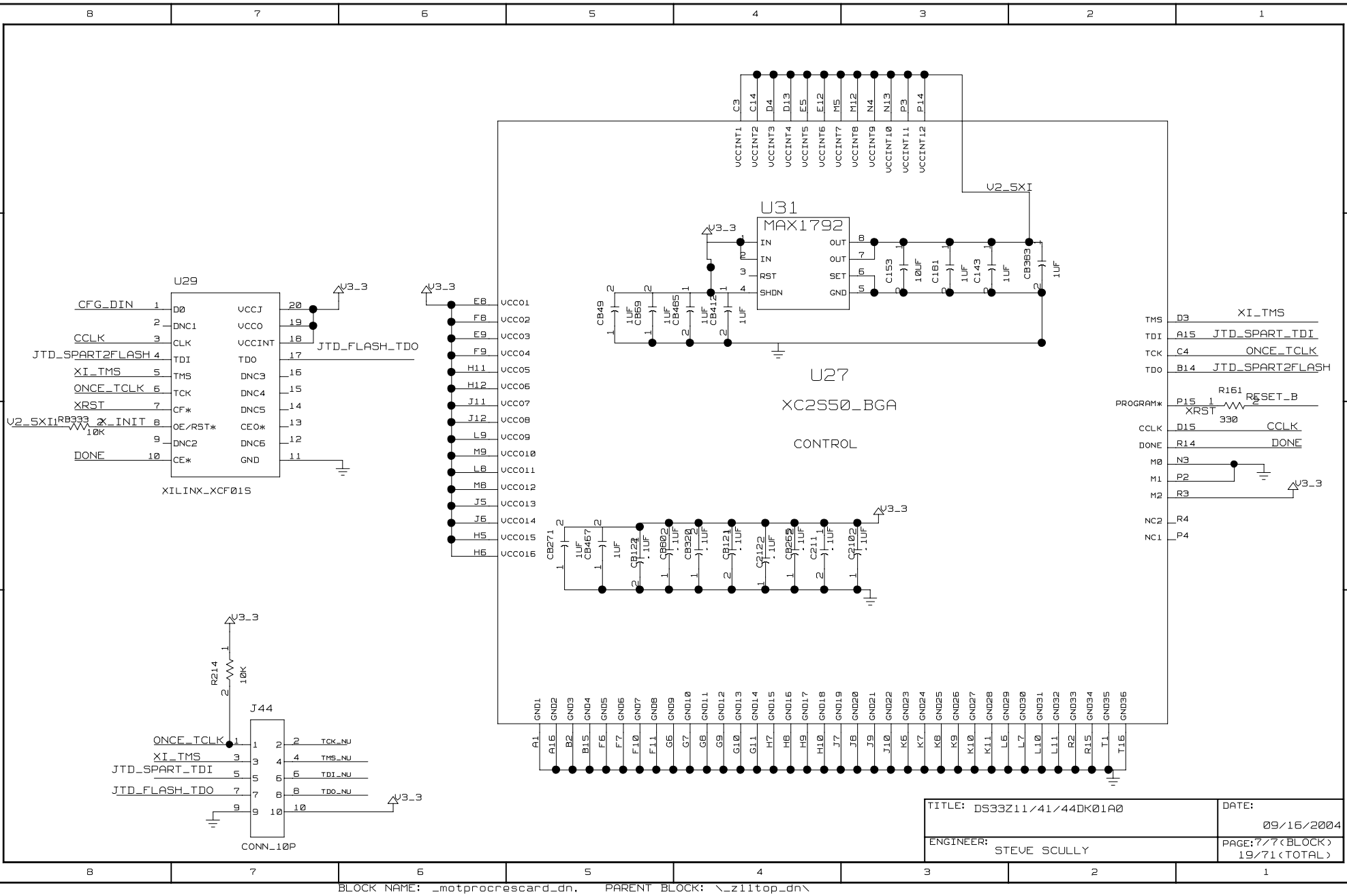
BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _zlltop_dn\





TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:6/7(BLOCK) 18/71(TOTAL)

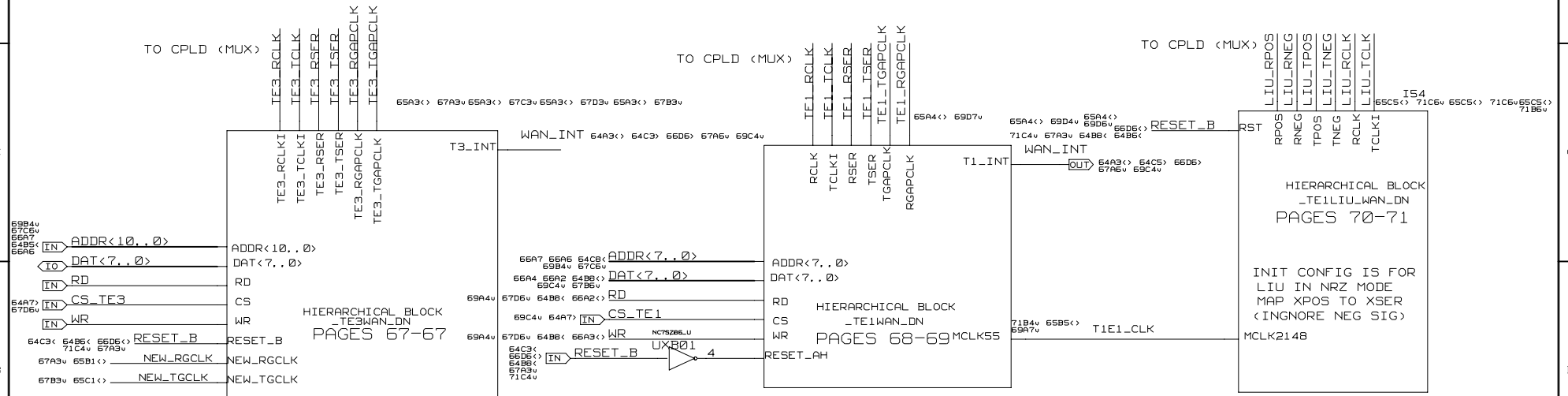
BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _zlltop_dn\



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 7/7 (BLOCK) 19/71 (TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _z11top_dn\

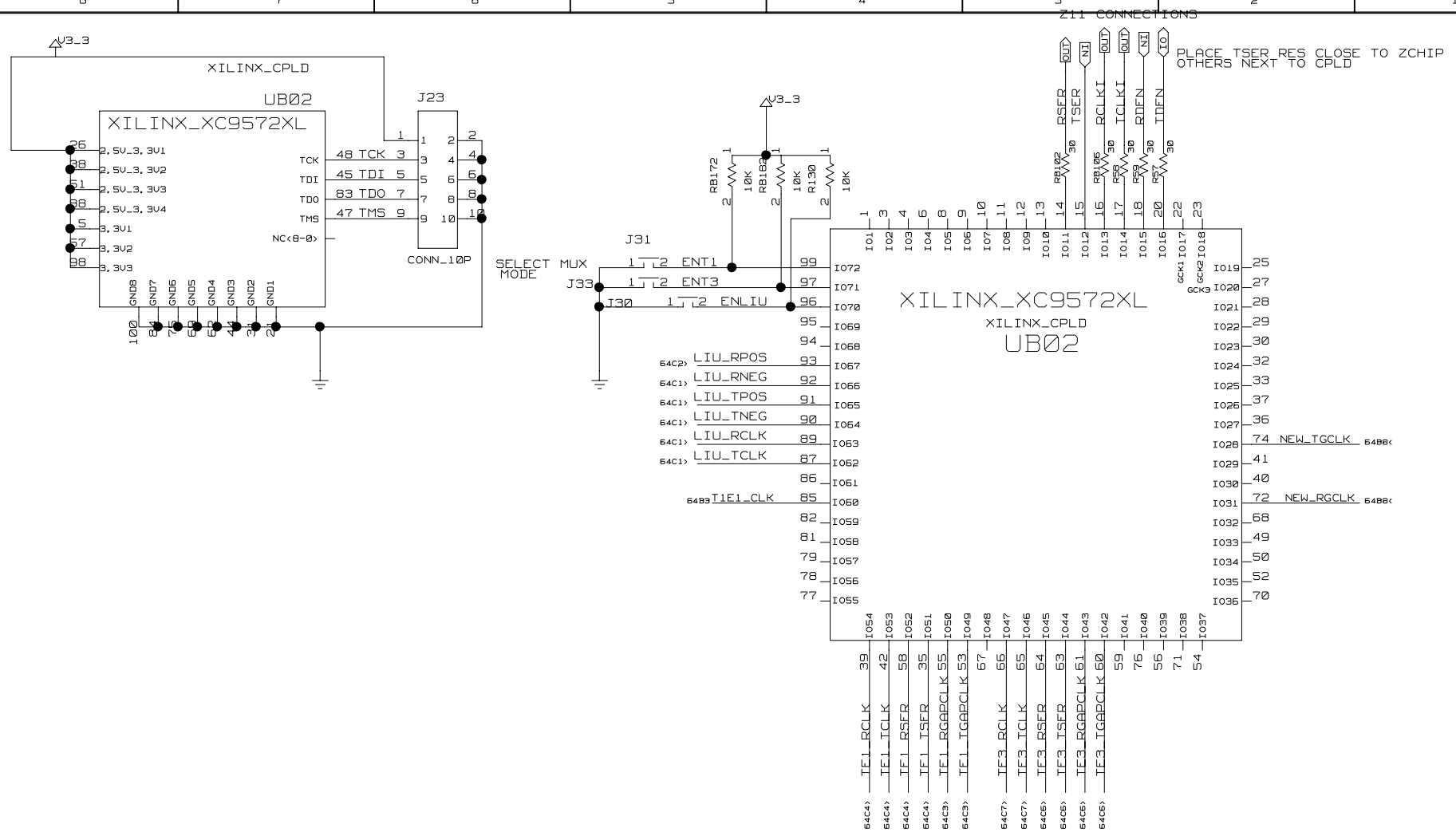
DS33Z11 WAN INTERFACE BLOCK



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:1/3‹BLOCK› 64/71‹TOTAL›

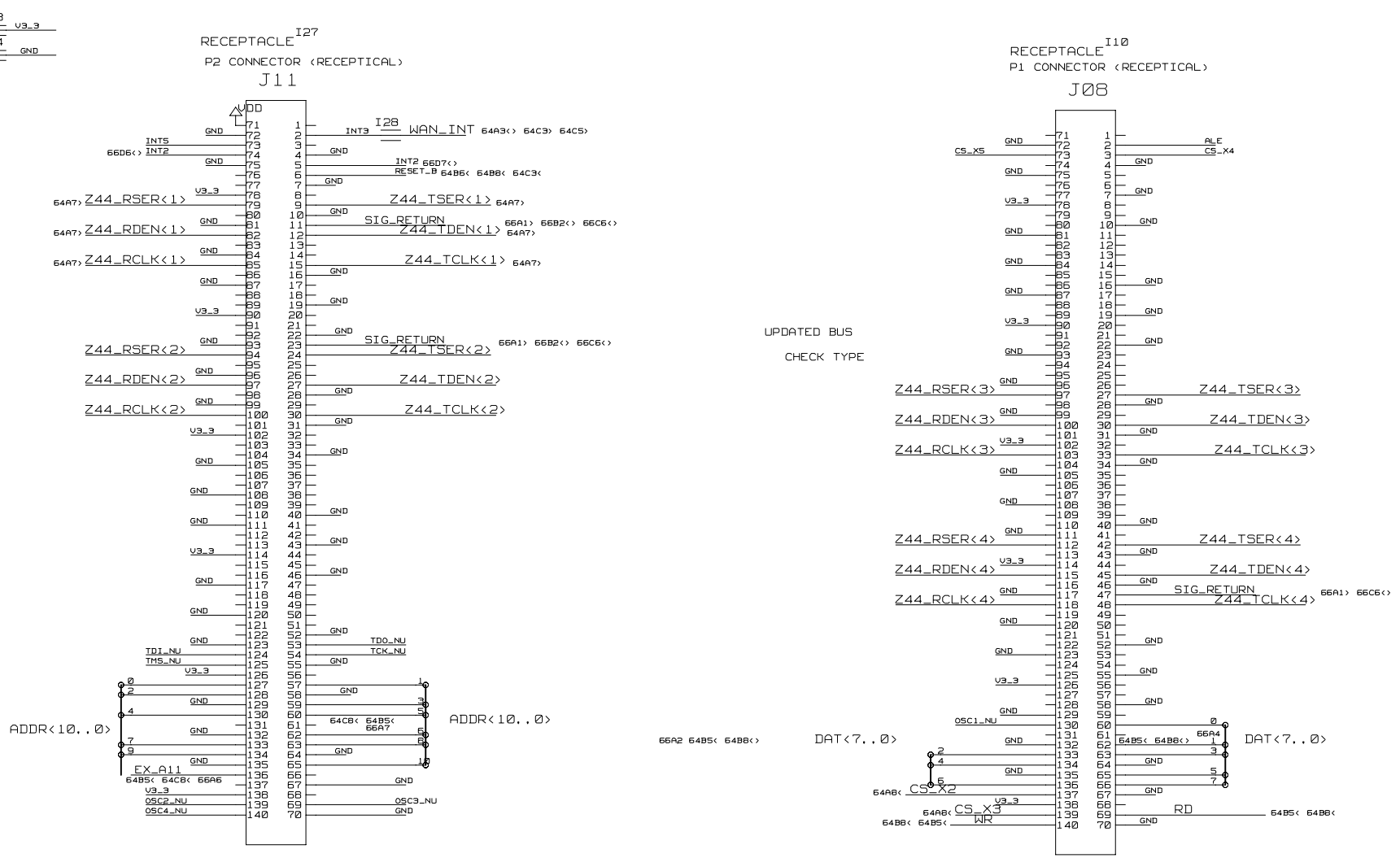
BLOCK NAME: _wan4z11_dn, PARENT BLOCK: _wan4z44_dn\

PRINTED Tue Feb 01 14:17:45 2005



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:2/3(BLOCK) 65/71(TOTAL)

BLOCK NAME: _wan4z11_dn, PARENT BLOCK: _wan4z44_dn\



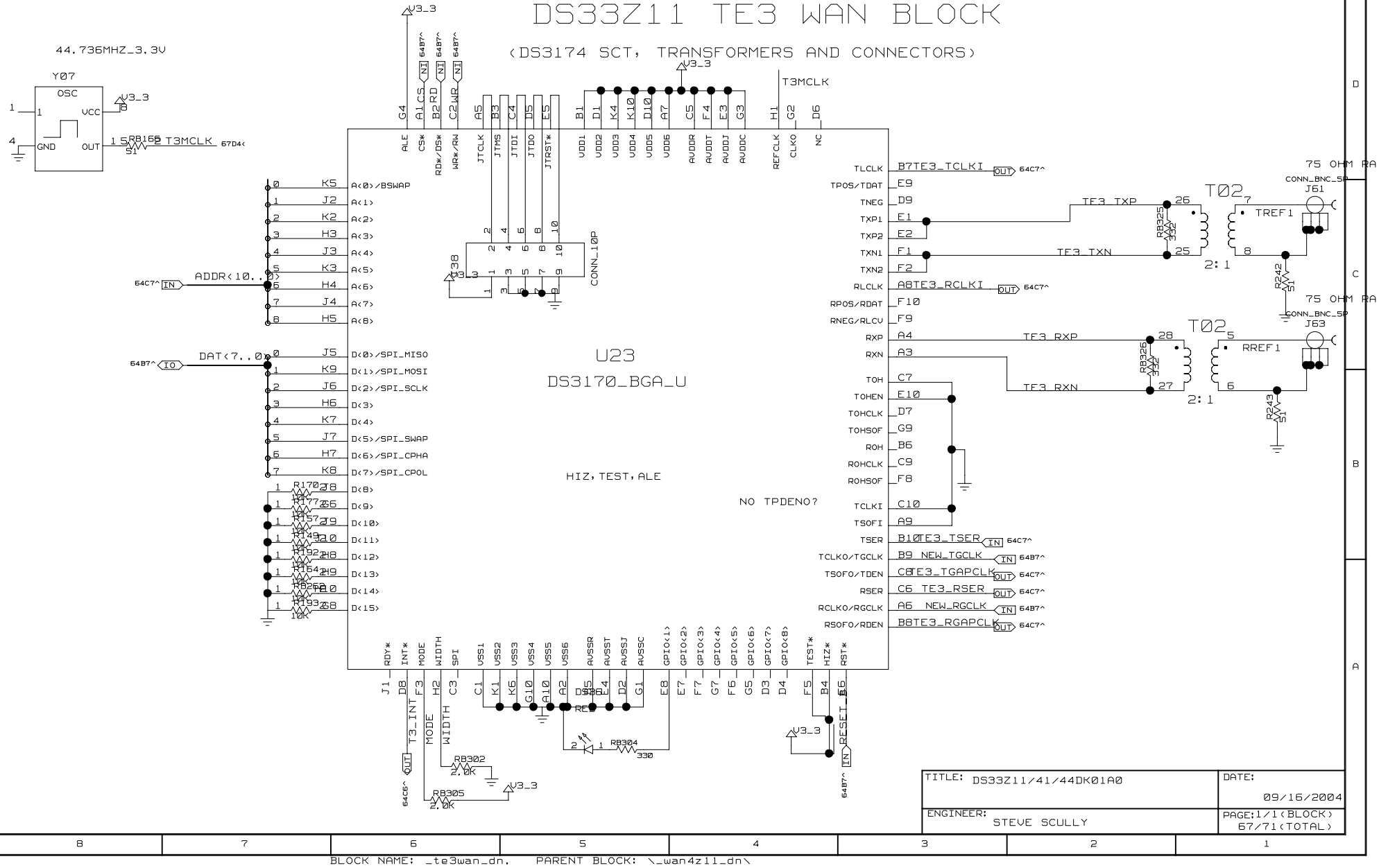
WAN R.C. CONNECTOR TO MOTHERBOARD

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:3/3(BLOCK) 66/71(TOTAL)

BLOCK NAME: _wan4z11_dn, PARENT BLOCK: _wan4z44_dn\

DS33Z11 TE3 WAN BLOCK

(DS3174 SCT, TRANSFORMERS AND CONNECTORS)

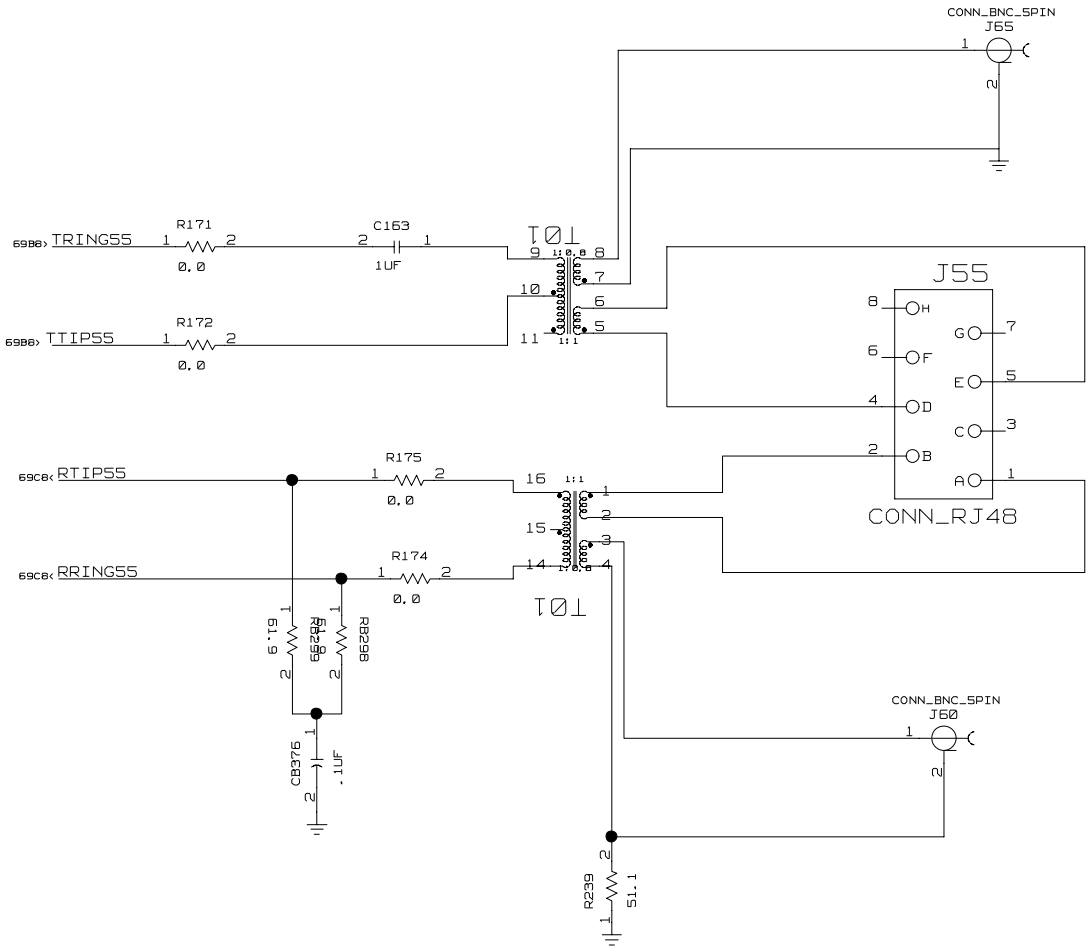


TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:1/1(BLOCK) 67/71(TOTAL)

BLOCK NAME: _te3wan_dn, PARENT BLOCK: _wan4z11_dn\

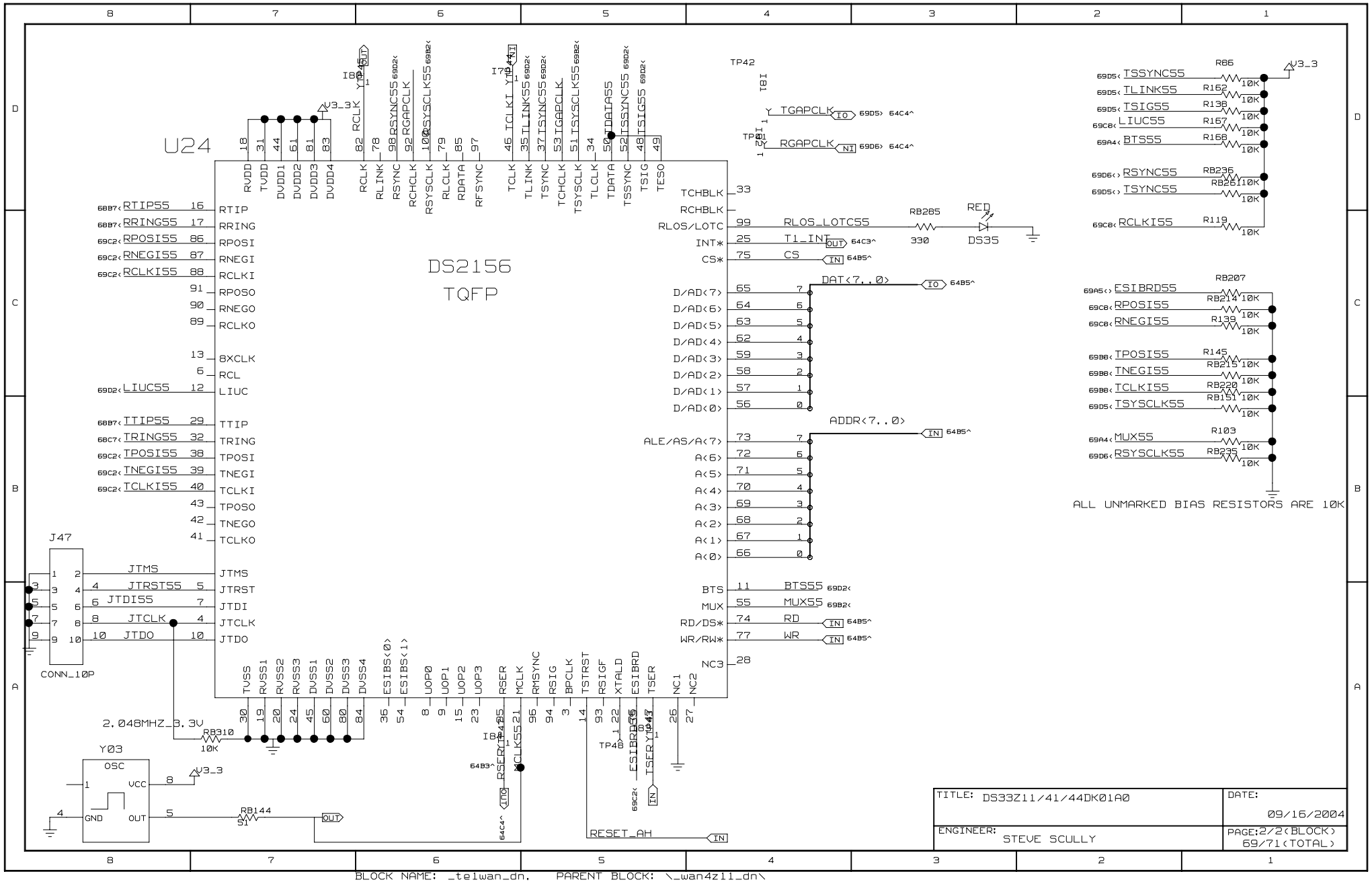
CR-68 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\,_WAN4Z44_DN\(SCH_1):PAGE1_I4@_ZTOP_LIB\,_WAN4Z11_DN\(SCH_1):PAGE1_I22@_ZTOP_LIB\,_TE1WAN_DN\(SCH_1):PAGE1

TE1 SINGLE WAN BLOCK



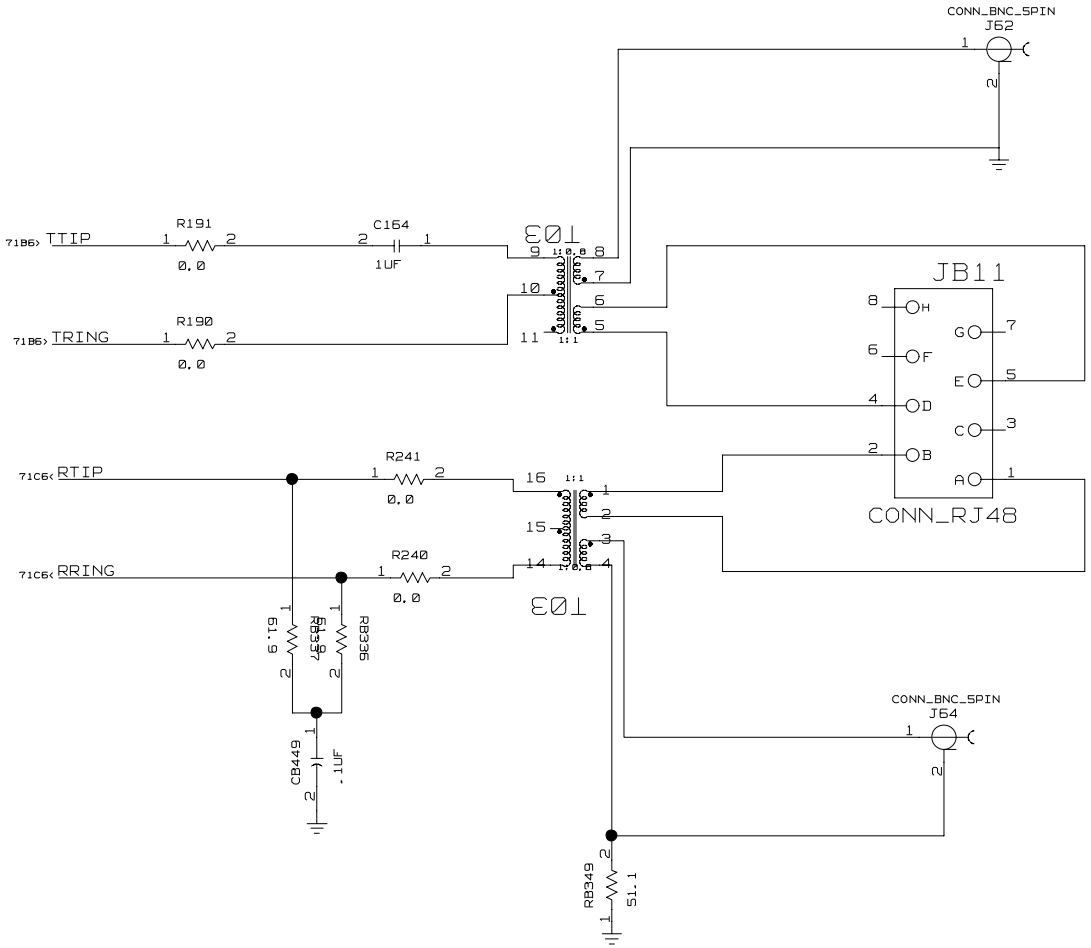
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:1/2(BLOCK) 68/71(TOTAL)

BLOCK NAME: _te1wan_dn, PARENT BLOCK: _wan4z11_dn\



BLOCK NAME: _te1wan_dn, PARENT BLOCK: _wan4z11_dn\

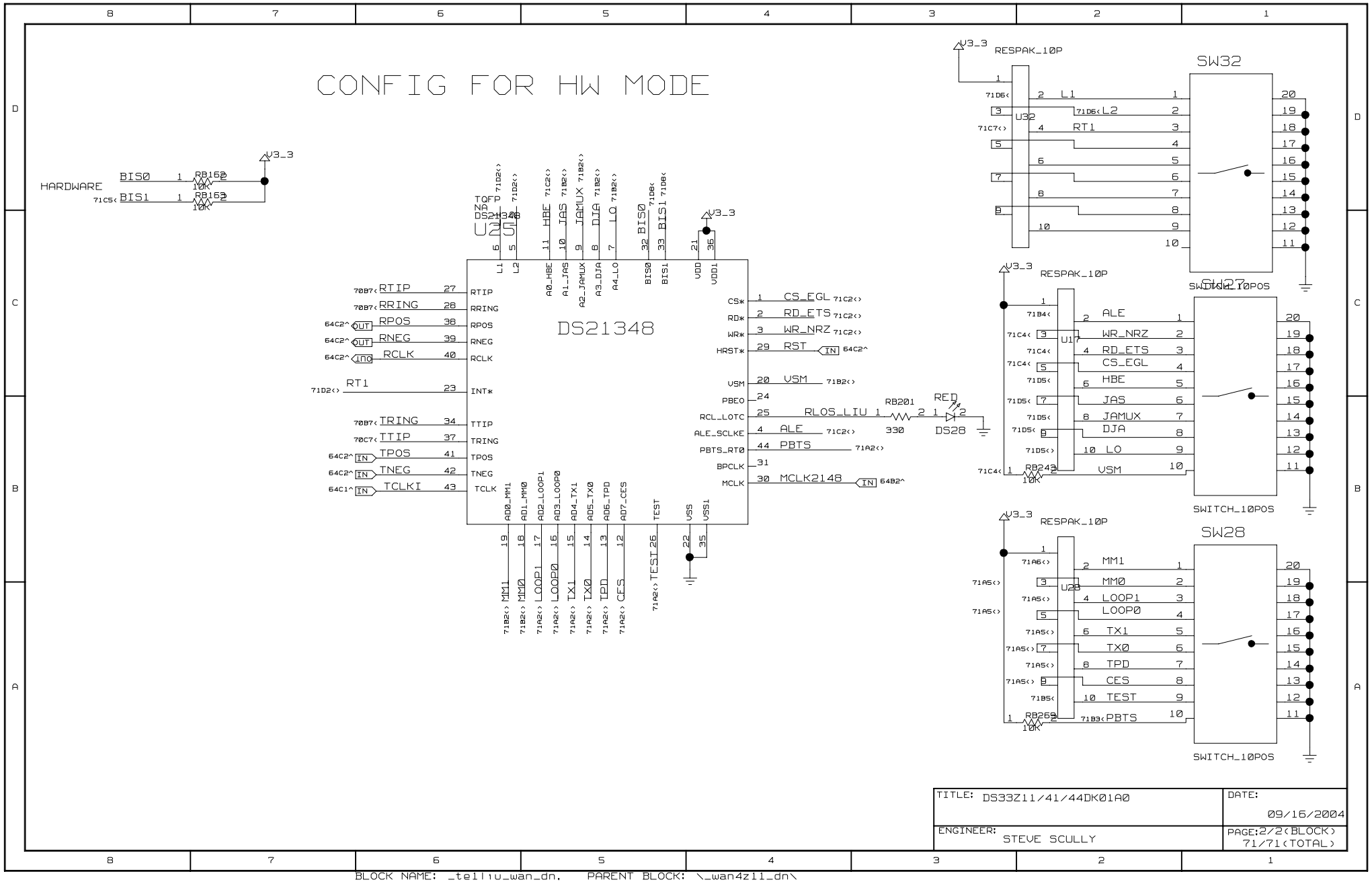
DS21348 LIU BLOCK



TITLE: DS33Z11/41/44DK01A0	DATE: 09/15/2004
ENGINEER: STEVE SCULLY	PAGE:1/2(BLOCK) 70/71(TOTAL)

BLOCK NAME: _te1liu_wan_dn, PARENT BLOCK: _wan4z11_dn\

CR-71 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\,_WAN4Z44_DN\(SCH_1):PAGE1_I4@_ZTOP_LIB\,_WAN4Z11_DN\(SCH_1):PAGE1_I54@_ZTOP_LIB\,_TE1LIU_WAN_DN\(SCH_1):PAGE2



BLOCK NAME: _te1liu_wan_dn, PARENT BLOCK: _wan4z11_dn\